1. Description

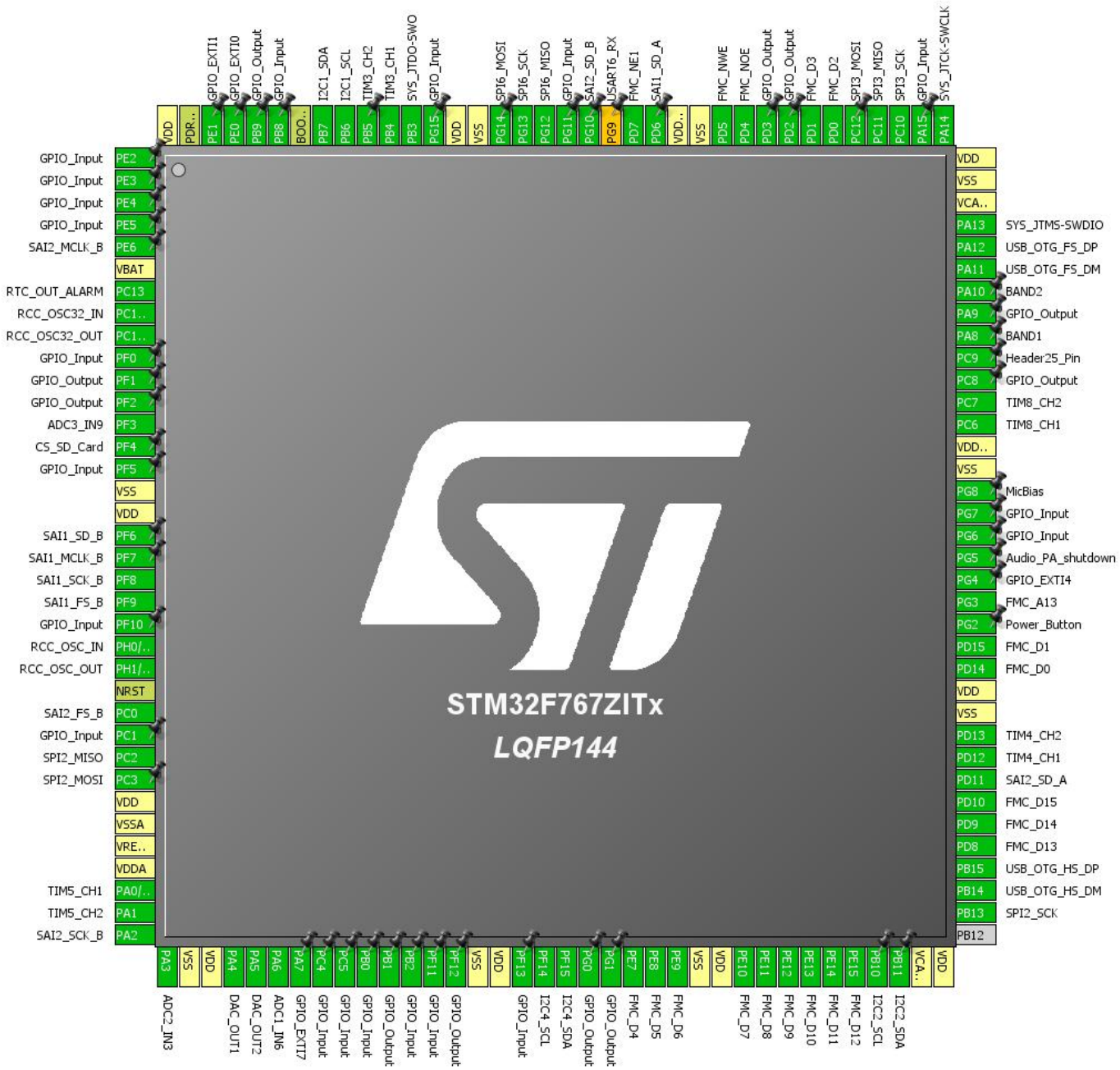
1.1. Project

Project Name	mchf15
Board Name	mchf15
Generated with:	STM32CubeMX 4.19.0
Date	02/07/2017

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	
2	PE3 *	I/O	GPIO_Input	
3	PE4 *	I/O	GPIO_Input	
4	PE5 *	I/O	GPIO_Input	
5	PE6	I/O	SAI2_MCLK_B	
6	VBAT	Power		
7	PC13	I/O	RTC_OUT_ALARM	
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF0 *	I/O	GPIO_Input	
11	PF1 *	I/O	GPIO_Output	
12	PF2 *	I/O	GPIO_Output	
13	PF3	I/O	ADC3_IN9	
14	PF4 *	I/O	GPIO_Input	CS_SD_Card
15	PF5 *	I/O	GPIO_Input	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	SAI1_SD_B	
19	PF7	I/O	SAI1_MCLK_B	
20	PF8	I/O	SAI1_SCK_B	
21	PF9	I/O	SAI1_FS_B	
22	PF10 *	I/O	GPIO_Input	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	SAI2_FS_B	
27	PC1 *	I/O	GPIO_Input	
28	PC2	I/O	SPI2_MISO	
29	PC3	I/O	SPI2_MOSI	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	TIM5_CH1	
35	PA1	I/O	TIM5_CH2	
36	PA2	I/O	SAI2_SCK_B	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
37	PA3	I/O	ADC2_IN3	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC_OUT1	
41	PA5	I/O	DAC_OUT2	
42	PA6	I/O	ADC1_IN6	
43	PA7	I/O	GPIO_EXTI7	
44	PC4 *	I/O	GPIO_Input	
45	PC5 *	I/O	GPIO_Input	
46	PB0 *	I/O	GPIO_Input	
47	PB1 *	I/O	GPIO_Output	
48	PB2 *	I/O	GPIO_Input	
49	PF11 *	I/O	GPIO_Input	
50	PF12 *	I/O	GPIO_Output	
51	VSS	Power		
52	VDD	Power		
53	PF13 *	I/O	GPIO_Input	
54	PF14	I/O	I2C4_SCL	
55	PF15	I/O	I2C4_SDA	
56	PG0 *	I/O	GPIO_Output	
57	PG1 *	I/O	GPIO_Output	
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	
66	PE13	I/O	FMC_D10	
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
69	PB10	I/O	I2C2_SCL	
70	PB11	I/O	I2C2_SDA	
71	VCAP_1	Power		
72	VDD	Power		
74	PB13	I/O	SPI2_SCK	
75	PB14	I/O	USB_OTG_HS_DM	
76	PB15	I/O	USB_OTG_HS_DP	

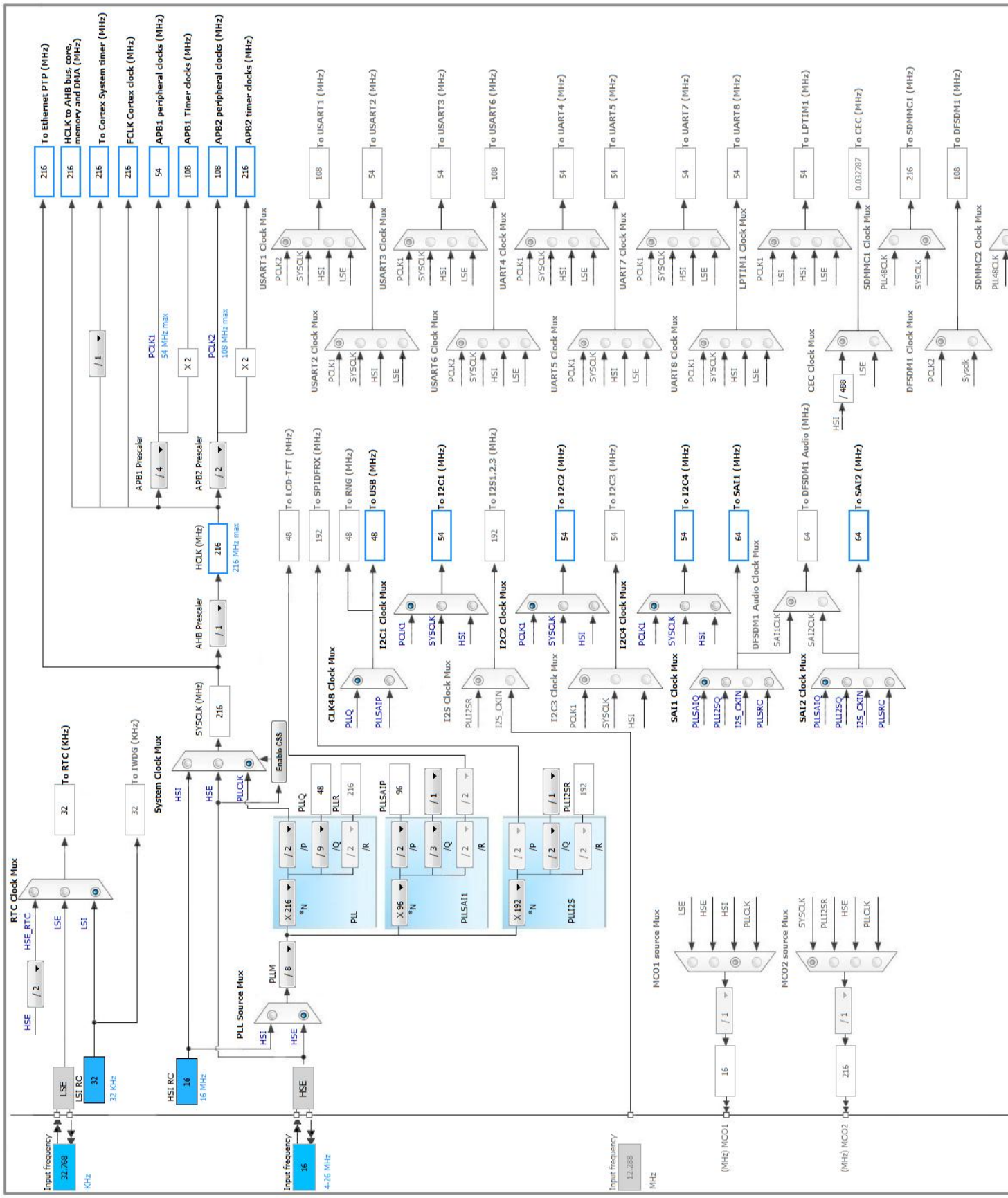
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
80	PD11	I/O	SAI2_SD_A	
81	PD12	I/O	TIM4_CH1	
82	PD13	I/O	TIM4_CH2	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
87	PG2	I/O	GPIO_EXTI2	Power_Button
88	PG3	I/O	FMC_A13	
89	PG4	I/O	GPIO_EXTI4	
90	PG5 *	I/O	GPIO_Output	Audio_PA_shutdown
91	PG6 *	I/O	GPIO_Input	
92	PG7 *	I/O	GPIO_Input	
93	PG8 *	I/O	GPIO_Output	MicBias
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	TIM8_CH1	
97	PC7	I/O	TIM8_CH2	
98	PC8 *	I/O	GPIO_Output	
99	PC9 *	I/O	GPIO_Output	Header25_Pin
100	PA8 *	I/O	GPIO_Output	BAND1
101	PA9 *	I/O	GPIO_Output	
102	PA10 *	I/O	GPIO_Output	BAND2
103	PA11	I/O	USB_OTG_FS_DM	
104	PA12	I/O	USB_OTG_FS_DP	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
110	PA15 *	I/O	GPIO_Input	
111	PC10	I/O	SPI3_SCK	
112	PC11	I/O	SPI3_MISO	
113	PC12	I/O	SPI3_MOSI	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
116	PD2 *	I/O	GPIO_Output	
117	PD3 *	I/O	GPIO_Output	
118	PD4	I/O	FMC_NOE	
119	PD5	I/O	FMC_NWE	
120	VSS	Power		
121	VDDSDMMC	Power		
122	PD6	I/O	SAI1_SD_A	
123	PD7	I/O	FMC_NE1	
124	PG9 **	I/O	USART6_RX	
125	PG10	I/O	SAI2_SD_B	
126	PG11 *	I/O	GPIO_Input	
127	PG12	I/O	SPI6_MISO	
128	PG13	I/O	SPI6_SCK	
129	PG14	I/O	SPI6_MOSI	
130	VSS	Power		
131	VDD	Power		
132	PG15 *	I/O	GPIO_Input	
133	PB3	I/O	SYS_JTDO-SWO	
134	PB4	I/O	TIM3_CH1	
135	PB5	I/O	TIM3_CH2	
136	PB6	I/O	I2C1_SCL	
137	PB7	I/O	I2C1_SDA	
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Input	
140	PB9 *	I/O	GPIO_Output	
141	PE0	I/O	GPIO_EXTI0	
142	PE1	I/O	GPIO_EXTI1	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN6

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 6
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN3

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 3
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. ADC3

mode: IN9

5.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 9
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.4. DAC

mode: OUT1 Configuration

mode: OUT2 Configuration

5.4.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None

5.5. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: LCD Interface

LCD Register Select: A13

Data: 16 bits

5.5.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	LCD Interface
Bank	Bank 1 NOR/PSRAM 1

Write operation	Enabled
Write FIFO	Enabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	255
Bus turn around time in HCLK clock cycles	15

5.6. I2C1

I2C: I2C

5.6.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.7. I2C2

I2C: I2C

5.7.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0

Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.8. I2C4

I2C: I2C

5.8.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.9. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.9.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.10. RTC

mode: Activate Clock Source

mode: Activate Calendar

Alarm A: Routed to OUT

WakeUp: Internal WakeUp

5.10.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255
Output Polarity	Output Polarity High
Output Type	Output Type Opendrain

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1

Year	0

Alarm A:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

Wake UP:

Wake Up Clock	RTCCLK / 16
Wake Up Counter	0

5.11. SAI1

Mode: Synchronous Slave

mode: I2S/PCM Protocol

Mode: Master with Master Clock Out

mode: I2S/PCM Protocol

5.11.1. Parameter Settings:

SAI A:

Basic Parameters	
Audio Mode	Slave Receive
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Protocol Parameters	
Protocol	I2S Standard
Data Size	16 Bits
Number of Slots (only Even Values)	2
Clock Parameters	
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	Disabled

Synchronization External	Disabled

SAI B:

Basic Parameters	
Audio Mode	Master Transmit
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Protocol Parameters	
Protocol	I2S Standard
Data Size	16 Bits
Number of Slots (only Even Values)	2
Clock Parameters	
Master Clock Divider	Enabled
Audio Frequency	192 KHz
Real Audio Frequency	0
Error between Selected	0
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	Disabled
Synchronization External	Disabled

5.12. SAI2

Mode: Synchronous Slave
mode: I2S/PCM Protocol
Mode: Master with Master Clock Out
mode: I2S/PCM Protocol

5.12.1. Parameter Settings:

SAI A:

Basic Parameters	
Audio Mode	Slave Receive
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Protocol Parameters	
Protocol	I2S Standard
Data Size	16 Bits
Number of Slots (only Even Values)	2

Clock Parameters	
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	Disabled
Synchronization External	Disabled

SAI B:

Basic Parameters	
Audio Mode	Master Transmit
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Protocol Parameters	
Protocol	I2S Standard
Data Size	16 Bits
Number of Slots (only Even Values)	2
Clock Parameters	
Master Clock Divider	Enabled
Audio Frequency	192 KHz
Real Audio Frequency	0
Error between Selected	0
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	Disabled
Synchronization External	Disabled

5.13. SPI2

Mode: Full-Duplex Master

5.13.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**27.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

5.14. SPI3

Mode: Full-Duplex Master

5.14.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**27.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

5.15. SPI6

Mode: Full-Duplex Master

5.15.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**54.0 MBits/s ***

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

5.16. SYS

Debug: Trace Asynchronous Sw

Timebase Source: SysTick

5.17. TIM3

Combined Channels: Encoder Mode

5.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.18. TIM4

Combined Channels: Encoder Mode

5.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.19. TIM5

Combined Channels: Encoder Mode

5.19.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0

Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.20. TIM8

Combined Channels: Encoder Mode

5.20.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct

Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.21. USB_OTG_FS

Mode: Device_Only

5.21.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Disabled

5.22. USB_OTG_HS

Internal FS Phy: Host_Only

5.22.1. Parameter Settings:

Speed	Host Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Physical interface	Internal Phy
Signal start of frame	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA3	ADC2_IN3	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PF3	ADC3_IN9	Analog mode	No pull-up and no pull-down	n/a	
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	
FMC	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG3	FMC_A13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C4	PF14	I2C4_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PF15	I2C4_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
RTC	PC13	RTC_OUT_ALARM	n/a	n/a	n/a	
SAI1	PF6	SAI1_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF7	SAI1_MCLK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF8	SAI1_SCK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF9	SAI1_FS_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SAI2	PE6	SAI2_MCLK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC0	SAI2_FS_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	SAI2_SCK_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD11	SAI2_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG10	SAI2_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI6	PG12	SPI6_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG13	SPI6_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PG14	SPI6_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PA0/WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
USB_OTG_HS	PB14	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB15	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
Single Mapped Signals	PG9	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
GPIO	PE2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PE5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CS_SD_Card
	PF5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA7	GPIO_EXTI7	External Interrupt Mode with	No pull-up and no pull-down	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
			Rising edge trigger detection			
	PC4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PF12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	Power_Button
	PG4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PG5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Audio_PA_shutdown
	PG6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MicBias
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Header25_Pin
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BAND1
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BAND2
	PA15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PE1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD interrupt through EXTI line 16	unused		
RTC wake-up interrupt through EXTI line 22	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line0 interrupt	unused		
EXTI line1 interrupt	unused		
EXTI line2 interrupt	unused		
EXTI line4 interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
EXTI line[9:5] interrupts	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI2 global interrupt	unused		
RTC alarms (A and B) interrupt through EXTI line 17	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
TIM5 global interrupt	unused		
SPI3 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
USB On The Go FS global interrupt	unused		
USB On The Go HS End Point 1 Out global	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
interrupt			
USB On The Go HS End Point 1 In global interrupt	unused		
USB On The Go HS global interrupt	unused		
FPU global interrupt	unused		
SPI6 global interrupt	unused		
SAI1 global interrupt	unused		
SAI2 global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev3

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	mchf15
Project Folder	G:\32f7\mchf15
Toolchain / IDE	Other Toolchains (GPDSC)
Firmware Package Name and Version	STM32Cube FW_F7 V1.6.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No