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Tx IQ Correction

Analogue IQ Error Correction For Transmitters - Off Line Method

1. Introduction

Direct conversion (IQ to RF) architectures based on Analogue IQ Modulators offer a low cost, relatively simple approach to radio communication transmitters. The required modulation information is first converted to equivalent "In phase" I_t and "Quadrature phase" Q_t signals containing all the required signal information. The spectrum of this IQ signal is usually centered at DC and is interpreted as having positive (+ = upper sideband) and negative (- = lower sideband) spectral components.

Compared to Direct RF Signal Synthesis (DRFSS) or IF to RF conversion based on a Superhet transmitter architecture, Direct Conversion offers a considerable reduction in hardware cost and complexity. The Digital To Analogue (ADC) converters used to generate I and Q signals only need to sample at twice the upper I or Q spectral component energy to correctly digitize the wanted transmit information prior to IQ to RF conversion. Even if "over-sampling" is used to alleviate the performance requirements of post ADC anti-alias rejection filters, the actual sample rate is much lower than the requirements of DAC to IF generation (superhet approach) or direct DAC to RF generation (DRFSS).

For example, consider a microwave QAM transmitter with a transmit spectral bandwidth requirement of ±1.5 MHz and a final output frequency of 2.65 GHz. A Direct Conversion IQ to RF conversion architecture will require each I and Q DAC to have a sample update rate of at least 3.0 MHz, and 10 MHz sampling rate would be reasonable. This I and Q "Complex Baseband" information would then be converted directly to the required RF frequency of 2.65 GHz using an Analogue IQ Modulator (IC or DBM) with a single LO input frequency also at 2.65 GHz.

In contrast, an IF to RF superhet approach would probably require two frequency conversions. For example,

DAC_IF Output @ 10 MHz IF_1 -> IF_2 @ 325 MHz -> RF Output at 2.65 GHz

The minimum DAC sample rate would be 20 MHz, but it would be preferable to over-sample at (say) 65 MHz or higher. High speed, high resolution DAC's increase sharply in price compared to their lower sampling rate cousins. Even if the difference is slight, the additional cost and complexity of a dual conversion superhet transmitter is unattractive. (requires two LO frequency synthesizers, two up conversion mixers and associated image and LO leakage reject filtering).

The DRFSS approach is probably infeasible at such frequencies based on today's DAC technology (and the speed of FPGA interface logic). A DAC would need to sample at least at 5.5 GHz to reconstruct this RF signal output (although an alias output could be used, as in sub-sampling, sample and hold based DAC's have a sinc{x} frequency roll-off characteristic and impaired linearity when used in a sub-sampling mode).

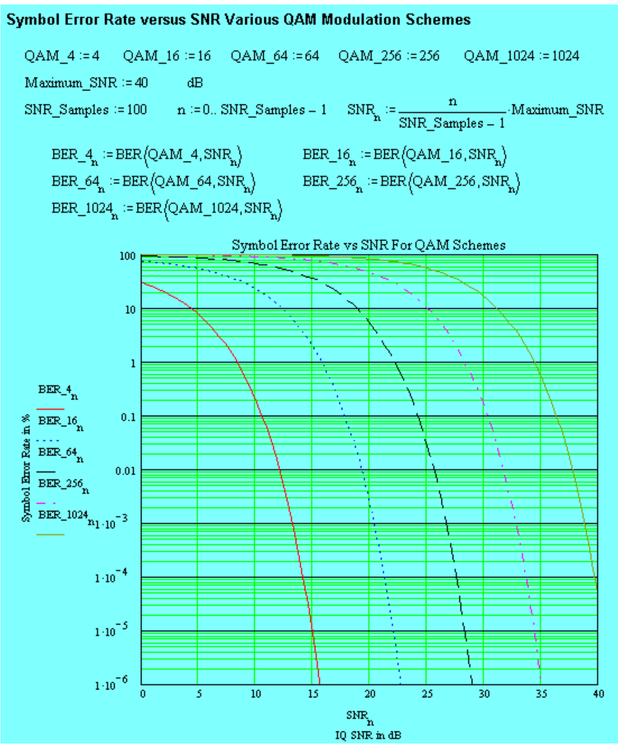
The Direct Conversion IQ to RF architecture certainly appears welcome in comparison! However this method has some (potential) limitations,

- Finite IQ linearity resulting in potential "spectral re-growth" - extending actual occupied RF bandwidth.
- Transmit Broad Band Noise - elevates overall background noise floor over a wide frequency range
- Residual LO to RF Carrier Leakage - causes a Signal to Noise Ratio (SNR) impairment.
- Spectral "Spillover" between upper + and lower - sideband components of the transmitted signal.

The first linearity impairment is usually solved by operating the IQ Modulator at a reduced IQ drive level. Usually 5dB to 10 dB "drive back-off" will be adequate. Some IQ modulators (e.g. Analog Devices AD) have internal IQ linearisation built in to reduce the need for IQ drive reduction. Improvements in device technology is on going. The issue of broad band noise is also being addressed. Early IQ modulators had broad band noise floors as high as -130 dB_{1Hz}! Modern IQ modulators can offer broad band noise floors better than -170 dB_{1Hz}.

(Note - some IQ modulators are specified with noise output in the absence of IQ drive. This can be misleading as broad band noise can increase by 10dB or more when modulation is applied to an Analogue IQ Modulator IC)

The last two imperfections show some improvement with technology advances but are likely to remain as potential weaknesses and contribute to a degradation in Signal To Noise Ratio (SNR) associated with the transmitted modulation. These IQ errors can present a SNR "floor" as low as 30 dB. To illustrate the importance of this, I have run a simple MATHCAD simulation for various levels of Quadrature Amplitude Modulation (QAM) based on some (admittedly) approximate mathematics!



Note: I have used actual RF SNR as the "x" variable as opposed to "Energy per bit" definitions. The actual RF bandwidth is centered around the RF carrier (at f_{LO}) and has twice the occupied bandwidth of I and Q channel spectral energy ($BW_{RF} = 2 * BW_I = 2 * BW_Q$).

The good news is that the Analog IQ errors can be corrected completely at IQ Baseband (in the digital domain). My article (following) shows exactly how this can be accomplished.

A simple method is described, based on a family of 8 IQ DC test vectors and monitoring the resulting RF envelope signal (e.g. with a simple diode detector). Variations in the envelope voltages are used to infer each IQ error. The inverse error correction mechanism is then applied in the digital domain thereby canceling the overall IQ errors out.

The errors targeted by this "off line" method are

- I DC Offset Imbalance - causes carrier leakage
- Q DC Offset Imbalance - also causes carrier leakage
- Relative IQ Gain Imbalance - causes spectral "spillover" between upper + and lower - sideband components of the transmitted signal.
- Relative LO Phase Skew Imbalance - also causes spectral "spillover" between upper + and lower - sideband components of the transmitted signal.

The method is applied iteratively until all errors are cancelled to an adequate level. This procedure is applied "off-air" and infrequently (IQ errors tend to be very stable over time). After satisfactory convergence is obtained, the IQ corrected transmitter is allowed to transmit actual RF signals with exceptional modulation accuracy.

Note: I have also developed an "on-line" error correction strategy that I will describe soon.

2.Deriving The Analogue IQ Error Correction Algorithm

2.1. How to Estimate IQ DC Offset Errors Based On A Model Based Parameter Extraction Method.

All Analogue IQ Modulators exhibit some carrier leakage from their Local Oscillator (LO) input to their RF output port. This has the effect of degrading in band Signal To Noise Ratio (SNR) performance on transmit. For example, residual LO carrier leakage at -40 dB from the wanted modulated output is equivalent to an in band SNR of 40 dB. The Bit Error Rate (BER) performance of high level QAM (e.g. QAM32 and higher) may be adversely affected by SNR noise floors around these levels.

LO carrier leakage arises from two main mechanisms,

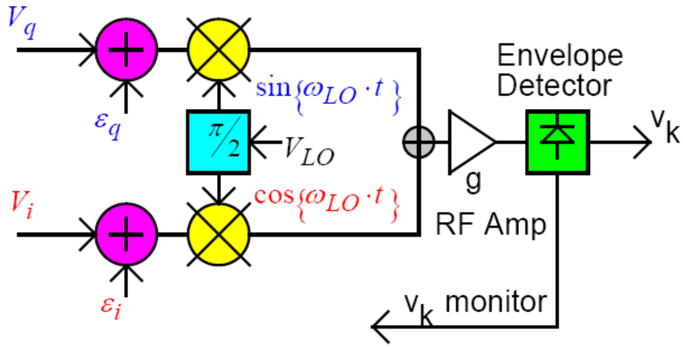
- Direct carrier leakage due to parasitic coupling between elements inside and surrounding the IQ Modulator.
- Inexact gain and phase matching between mixing elements contained in the internal Double Balanced Mixers (DBM) - An Analogue IQ modulator contains two such mixers driven with a quadrature phase LO.
- Inexact DC offset cancellation at the IF port of each internal DBM.

Although the mechanisms may be different, all are functionally equivalent to the presence of DC offset errors at the I and Q input ports of the Analogue IQ modulator. It follows then, that if an equal and opposite I and Q DC offset voltage is applied to these ports, the resulting LO to RF leakage will be cancelled to zero.

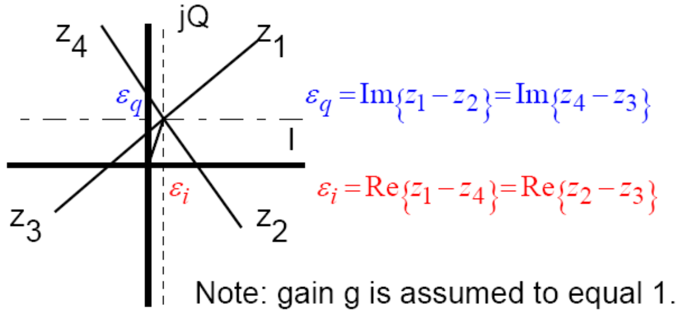
This next diagram and associated mathematics shows a model for LO to RF leakage "referred to IQ Baseband" as equivalent IQ DC offsets. A sequence of 4 IQ DC test vectors is used to infer these error from a measurement of the resulting envelope variations appearing at the IQ modulator's RF output (or after subsequent RF amplification).

IQ DC Offset Error Estimation And Correction

Analog IQ DC Offset Referred to Baseband



Graphical Interpretation For IQ DC Offset Error



Define $V_{iq} \equiv V_i + j \cdot V_q$ and $V_{iq}^{/} \equiv V_{iq} + \varepsilon_{iq}$ where $\varepsilon_{iq} \equiv \varepsilon_i + j \cdot \varepsilon_q$ ...(1)

Equation (1) represents the effect of a small IQ DC offset corresponding to the graphical illustration. This systematic error will cause predictable envelope error perturbations away from those expected from the (exact) IQ DC test vectors. These perturbation errors can be monitored using a simple diode detector placed somewhere in the RF path.

The ***detected RF envelope*** voltage v_k for each kth test vector can be represented as

$$v_k \equiv g \cdot \left[\sqrt{V_{i,k}{}^2 + V_{q,k}{}^2} \right] \ldots (2)$$

Here g represents the IQ to RF → DC_{diode} conversion gain of the system. When an IQ DC offset is introduced, the new predicted RF envelopes become

$$v_k \equiv g \cdot \left[\sqrt{(V_{i,k} + \varepsilon_i)^2 + (V_{q,k} + \varepsilon_q)^2} \right] \ldots (3)$$

Squaring both sides provides,

$$\begin{aligned} v_k{}^2 &\equiv g^2 \cdot \left[(V_{i,k} + \varepsilon_i)^2 + (V_{q,k} + \varepsilon_q)^2\right] \\ &= g^2 \cdot \left[V^2{}_{i,k} + 2 \cdot V_{i,k} \cdot \varepsilon_i + \varepsilon_i{}^2 + V^2{}_{q,k} + 2 \cdot V_{q,k} \cdot \varepsilon_q + \varepsilon_q{}^2\right] \end{aligned} \ldots(4)$$

The variation in the detected RF power (voltage squared) between these 2 test vector pairings is,

$$\begin{aligned} &v_k{}^2 \equiv g^2 \cdot \left[V^2{}_{i,k} + 2 \cdot V_{i,k}\varepsilon_i + \varepsilon_i{}^2 + V^2{}_{q,k} + 2 \cdot V_{q,k} \cdot \varepsilon_{iq} + \varepsilon_q{}^2\right] \\ &v_{k'}{}^2 \equiv g^2 \cdot \left[V^2{}_{i,k'} + 2 \cdot V_{i,k'}\varepsilon_i + \varepsilon_i{}^2 + V^2{}_{q,k'} + 2 \cdot V_{q,k'}\varepsilon_i + \varepsilon_q{}^2\right] \\ &\Rightarrow v_k{}^2 - v_{k'}{}^2 = 2 \cdot g^2 \cdot \left[\left(V_{i,k} - V_{i,k'}\right) \cdot \varepsilon_i + \left(V_{q,k} - V_{q,k'}\right) \cdot \varepsilon_q + \left(V_{i,k}^2 - V_{i,k'}^2\right) + \left(V_{q,k}^2 - V_{q,k'}^2\right)\right] \end{aligned} \ldots(5)$$

Let us define each test vector pair to have equal I magnitude and Q magnitude so that $V_{i,k}^2 - V_{i,k'}^2 \equiv 0 \; and \; V_{q,k}^2 - V_{q,k'}^2 \equiv 0$. Also let's define $\Delta v^2{}_{k,k'} \equiv v^2{}_k - v^2{}_{k'}$. Equation (5) now becomes

$$\Delta v_{k,k'}^2 = 2 \cdot g^2 \cdot \left[\left(V_{i,k} - V_{i,k'}\right) \cdot \varepsilon_i + \left(V_{q,k} - V_{q,k'}\right) \cdot \varepsilon_q\right] \ldots(6)$$

To further simplify, let's also define $\Delta V_{i,k,k'} \equiv V_{i,k} - V_{i,k'} \; and \; \Delta V_{q,k,k'} \equiv V_{q,k} - V_{q,k'}$. We can now write equation (6) as

$$\Delta v_{k,k'}^2 = 2 \cdot g^2 \cdot \left[\Delta V_{i,k,k'} \cdot \varepsilon_i + \Delta V_{q,k,k'} \cdot \varepsilon_q\right] \ldots(7)$$

Consequently the predicted IQ DC offset errors are,

$$\begin{aligned} \varepsilon_i &= \frac{1}{\Delta V_{i,k,k'}} \cdot \left(\frac{\Delta v^2{}_{k,k'}}{2 \cdot g^2} - \Delta V_{q,k,k'} \cdot \varepsilon_q\right) \\ \varepsilon_q &= \frac{1}{\Delta V_{q,k,k'}} \cdot \left(\frac{\Delta v^2{}_{k,k'}}{2 \cdot g^2} - \Delta V_{i,k,k'} \cdot \varepsilon_i\right) \end{aligned} \ldots(8)$$

We now need to "uncouple" the error term estimates by setting $\Delta V_{q,k,k'} \equiv 0$ but $\Delta V_{i,k,k'} \neq 0$ for the "I" channel error estimate. Also we will select $\Delta V_{i,k,k'} \equiv 0$ but $\Delta V_{q,k,k'} \neq 0$ for the "Q" channel error estimate (note – these are both ***real*** unlike $V_{iq,k,k'}$ which is ***complex***). The use of 4 IQ test vectors of unit magnitude spaced at 45, -45, -135 and 135 degrees seems most suitable,

Equation (8) shows how each I and Q DC offset can be derived from the measured RF envelope voltage combined with each k^{th} IQ test vector and a knowledge of the overall system gain "g" (which can always be scaled to a convenient value of one either in hardware or as a digital scale factor multiplication).

I and Q DC error estimates depend on each other, but suitable selection of I and Q test vectors can eliminate this dependency. The I DC offset error estimate requires two test vectors k and k' to have equal Q values and the Q DC offset error estimate requires The k and k' I values to be equal,

$$V_{iq,1}=\frac{1}{\sqrt{2}}\cdot(1+j)$$
$$V_{iq,2}=\frac{1}{\sqrt{2}}\cdot(1-j)$$
$$V_{iq,3}=\frac{1}{\sqrt{2}}\cdot(-1-j) \quad \ldots(9)$$
$$V_{iq,4}=\frac{1}{\sqrt{2}}\cdot(-1+j)$$

This results in a convenient outcome,

$$\Delta V_{i,1,2}=\Delta V_{q,2,3}=\Delta V_{i,3,4}=\Delta V_{q,4,1}=0$$
$$\Delta V_{q,1,2}=\Delta V_{i,2,3}=-\Delta V_{q,3,4}=-\Delta V_{i,4,1}=\sqrt{2} \quad \ldots(10)$$

The I DC offset error ε_i is best determined using test vector pairs [2,3] and/or [4,1] whilst the Q DC offset error ε_q can use test vector pairs [1,2] and [3,4]. Equation (8) becomes,

$$\varepsilon_i=\frac{\Delta v_{2,3}^2}{2\cdot\sqrt{2}\cdot g^2} \quad \text{or} \quad \varepsilon_i=-\frac{\Delta v_{4,1}^2}{2\cdot\sqrt{2}\cdot g^2} \quad \ldots(11)$$
$$\varepsilon_q=\frac{\Delta v_{1,2}^2}{2\cdot\sqrt{2}\cdot g^2} \quad \quad \varepsilon_q=-\frac{\Delta v_{3,4}^2}{2\cdot\sqrt{2}\cdot g^2}$$

Although either test vector pairing could be used for estimation purposes, better accuracy would be expected from taking an average of both estimates,

$$\bar{\varepsilon}_i=\frac{\Delta v_{2,3}^2+\Delta v_{1,4}^2}{4\cdot\sqrt{2}\cdot g^2} \;\&\; \bar{\varepsilon}_q=\frac{\Delta v_{1,2}^2+\Delta v_{4,3}^2}{4\cdot\sqrt{2}\cdot g^2} \quad \ldots(12)$$

<u>Note:</u> $\Delta v_{1,4}^2=-\Delta v_{4,1}^2$ etc

Alternatively we can rewrite equation (12) as

$$\bar{\varepsilon}_i=\frac{\left(v_1^2+v_2^2\right)-\left(v_3^2+v_4^2\right)}{4\cdot\sqrt{2}\cdot g^2} \;\&\; \bar{\varepsilon}_q=\frac{\left(v_1^2+v_4^2\right)-\left(v_2^2+v_3^2\right)}{4\cdot\sqrt{2}\cdot g^2} \quad \ldots(13)$$

<u>Worked Example</u>

We will assume that the transmitter has been designed with g ≡ 1 in mind, or the feedback envelope is scaled digitally to achieve the same result. It isn't critical that the loop gain is exactly equal to one, as it just scales the error estimate and this scaling error tends to zero as the IQ errors are removed.

The four IQ test vectors selected allow two estimates for I DC offset and two for Q DC offset. Averaging both dual estimates improves accuracy and results in a simple computation shown in equation (13). A worked example follows, using extremely high DC offset errors in order to demonstrate the method's robustness to error.

Let $\varepsilon_i = 0.1$, $\varepsilon_q = -0.15$ with $g \equiv 1$

k	V_{iq} Test Vector	V_{iq} + DC Error	$v_k^2 \equiv V_i^2 + V_q^2$	$\bar{\varepsilon}_i = \frac{\Delta v_{2,3}^2 + \Delta v_{1,4}^2}{4 \cdot \sqrt{2} \cdot g^2}$	$\bar{\varepsilon}_q = \frac{\Delta v_{1,2}^2 + \Delta v_{4,3}^2}{4 \cdot \sqrt{2} \cdot g^2}$
1	0.707 + j 0.707	0.807 + j 0.557	0.961	$\varepsilon_{i,2,3}$ = 0.1000556	$\varepsilon_{q,1,2}$ = -0.15026
2	0.707 – j 0.707	0.807 – j 0.857	1.386	$\varepsilon_{i,1,4}$ = 0.0997021	$\varepsilon_{i,4,3}$ = -0.14991
3	-0.707 – j 0.707	-0.607 - j 0.857	1.103		
4	-0.707 + j 0.707	-0.607 + j 0.557	0.679	**ε_i = 0.09988**	**ε_q = -0.15009**

The IQ DC offsets are estimated with excellent accuracy. The introduced I DC offset of 0.1 is estimated to be 0.09988 (an estimate error of only -0.00012 or -0.12%). The introduced Q DC offset of -0.15 is estimated to be -0.15009 (an estimate error of only 0.00009 or 0.06%). “I” and “Q” DC offset errors were introduced simultaneously, and both estimates (of these errors) show themselves to be independent of each other.

We also note that the IQ DC errors used for this demonstration are extremely high when compared with those found in typical IQ modulators. In practice, the IQ DC offsets can be expected to be far less than those used for demonstration, by a factor of 10:1 on average.

2.2. How to Estimate IQ Gain Imbalance Errors Based On A Model Based Parameter Extraction Method.

All Analogue IQ Modulators exhibit some cross coupling between upper and lower sideband energy at their RF output port. This is usually measured for a single IQ carrier input based on a cosine (I channel) and sine (Q channel) signal source.

Under these conditions, and "ideal" Analogue IQ modulator would produce a single RF output carrier with a frequency equal to the LO input frequency + the IQ sinusoidal tone frequency. If the Q channel polarity is inverted, the RF output carrier would equal the LO carrier frequency - the IQ sinusoidal modulating frequency.

Real Analog IQ modulators are not perfect (of course) and some residual "other sideband" RF carrier leakage will be observed. As in the case of LO carrier leakage this represents another in band SNR degradation mechanism. For example, a sideband suppression ratio of -40 dB from the wanted modulated output is equivalent to an in band SNR of 40 dB. When actual modulation is applied, spectral energy from upper and lower sideband regions will intermingle causing in band interference. The Bit Error Rate (BER) performance of high level QAM (e.g. QAM32 and higher) may then be adversely affected by this degraded SNR floor.

Two primary mechanisms are responsible for the intermingling between upper and lower spectral energy components,

- The Analog IQ Modulator has internal DBMs with slightly different conversion gains. This gain imbalance prevents exact cancellation of the unwanted sideband component.
- The Analog IQ Modulator an inexact phase quadrature LO source for each of its two internal DBMs. This "phase skew error" also prevents exact cancellation of the unwanted sideband component.

If one of the internal DBMs has a slightly different conversion gain, it is perfectly reasonable to expect that its I (or Q) drive is simply scaled up or down in level to compensate. This analysis assumes that one DBM will have high conversion gain, and the other will have lower conversion gain. This symmetry is mathematically convenient as it tends to preserve an average conversion gain.

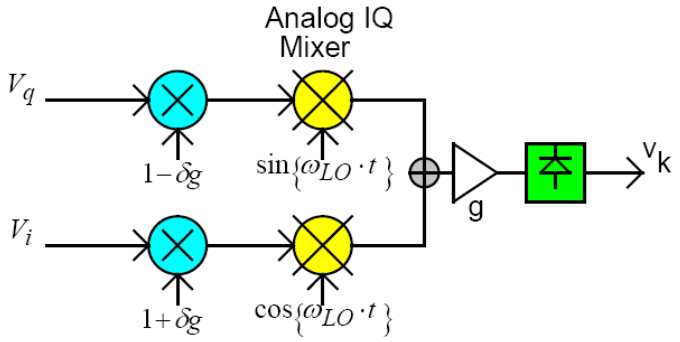
We will normalize average conversion gain "**g**" to unity for convenience, as this scaling can always be accomplished without effort. The individual I and Q conversion path gains will be represented as **g** = 1 ±*dg*.

Note: To be pedantically exact, the "I" correction gains should be be $g_I' = g_I / (1+dg)$ and the "Q" correction gain should be $g_Q' = g_q /(1-dg)$ but dg is assumed to be small so the binomial approximations 1/(1+*dg*) ~ 1-*dg* and 1/(1-*dg*) ~ 1+*dg* seem reasonable. Given that "division" is more computationally intensive than addition and subtraction this "purity" seems unjustifiable considering the minimal estimation error introduced. The importance of any such inaccuracy further diminishes as the gain imbalance error is removed (a relative gain imbalance only requires a single variable). The minor consequence of this approximation is to introduce a small global gain scale error. Since RF amplifiers have frequency and temperature dependent gain anyway, this global gain modification would be corrected by existing output power management and control systems anyway.

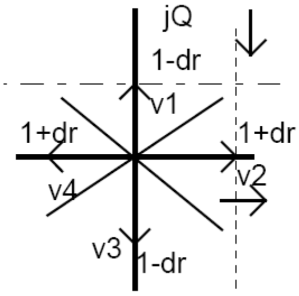
The next analysis shows the method for determining this gain imbalance, followed by another analysis showing how to derive phase skew errors in section 2.3.

IQ Gain Imbalance Error Estimation and Correction

IQ Relative Gain Imbalance Referred to Baseband



Geometrical View For IQ Gain Imbalance (for g=1)



$$\begin{bmatrix} V_i' \\ V_q' \end{bmatrix} = \begin{bmatrix} 1+\delta g & 0 \\ 0 & 1-\delta g \end{bmatrix} \cdot \begin{bmatrix} V_i \\ V_q \end{bmatrix}$$

Relative IQ gain imbalance uses a different set of IQ test vectors compared to the previous case of IQ DC offset error.

The ***relative*** IQ gain offset is represented as ∂g, and the ***absolute*** gain as g**.** The absolute gain g can be computed prior to the extraction of other parameters (derived from an average of all 8 measured RF DC voltages when a test vector magnitude of "1" is used).

i.e. $\tilde{g}^2 \approx \frac{1}{8} \cdot \sum_{k=1}^{8} v_k^2 \;\; providing \; \left|V_{iq}\right| \equiv 1 \; for \; all \; k \in [1,2,...,8]$ …(14)

(This initial normalization procedure would be expected anyway as providing a simple diagnostic for potential hardware faults).

We want to infer the relative gain imbalance parameter ∂g from RF envelope information, given that we first define suitable DC IQ training vectors.

$$\begin{aligned} v_k^2 &\equiv g^2 \cdot \left[V_{i,k}^2 \cdot (1+dg)^2 + V_{q,k}^2 \cdot (1-dg)^2\right] \\ &= g^2 \cdot \left[(V^2_{i,k} + V^2_{q,k}) \cdot (1+dg^2) + 2 \cdot V^2_{i,k} \cdot dg - 2 \cdot V^2_{q,k} \cdot dg\right] \end{aligned} \quad \text{…(15)}$$

Let us take 2 vectors k and k' from our test family and look at the difference in the measured RF envelope,

Let's assume that IQ gain imbalance will be relatively small, e.g. *dg* = 0.05 corresponding to an imbalance of ±0.4 dB (not impressive based on modern standards). The dg^2 term is therefore relatively insignificant and will be ignored. The relative difference between vector pairings k and k' becomes,

$$\begin{aligned} &\Delta v^2_{k,k'} = 2 \cdot g^2 \cdot \left(\Delta V^2_{i,k,k'} - \Delta V^2_{q,k,k'}\right) \cdot dg \\ &\text{where } \Delta V^2_{i,k,k'} \equiv V^2_{i,k} - V^2_{i,k'} \\ &\text{and } \Delta V^2_{q,k,k'} \equiv V^2_{q,k} - V^2_{q,k'} \qquad \text{...(16)} \\ &\Rightarrow dg = \frac{1}{2 \cdot g^2} \cdot \frac{\Delta v^2_{k,k'}}{\left(\Delta V^2_{i,k,k'} - \Delta V^2_{q,k,k'}\right)} \end{aligned}$$

Let us now define 2 "appropriate" test vectors,

$$\begin{aligned} &V_{i,5} \equiv 1, V_{q,5} \equiv 0 \\ &V_{i,6} \equiv 0, V_{q,6} \equiv 1 \\ &i.e.\, \Delta V^2_{i,5,6} = 1, \Delta V^2_{q,5,6} = -1, \qquad \text{...(17)} \\ &\text{(recall definition of } \Delta V^2_{i,k,k'} \; and \; \Delta V^2_{q,k,k'}) \end{aligned}$$

Since the difference in the denominator equals 2, equation (16) simplifies to,

$$dg_{5,6} = \frac{\Delta v^2_{5,6}}{4 \cdot g^2} \quad \text{...(18)}$$

Equation (18) shows how one IQ test vector pairing (k=5,6) can produce a gain imbalance estimate *dg*. However this estimate can also be obtained from 3 other possible pairings. Each estimate may suffer from various accuracy limitations, so it makes good engineering sense to assemble and average of all four, given that each estimate is no better or worse, on average, than the other.

We can use all four possible pairings of orthogonal test vectors, i.e.

$$dg_{5,6} = \frac{\Delta v_{5,6}^2}{4 \cdot g^2},\ dg_{5,8} = \frac{\Delta v_{5,8}^2}{4 \cdot g^2},\ dg_{7,6} = \frac{\Delta v_{7,6}^2}{4 \cdot g^2},\ dg_{3,4} = \frac{\Delta v_{7,8}^2}{4 \cdot g^2} \ldots (19)$$

Once again, these 4 IQ relative gain error estimates $dg_{k,k'}$ may be averaged to enhance overall estimation accuracy,

$$\bar{dg} \equiv \frac{\Delta v_{5,6}^2 + \Delta v_{5,8}^2 + \Delta v_{7,6}^2 + \Delta v_{7,8}^2}{16 \cdot g^2}$$

$$\Rightarrow \bar{dg} \equiv \frac{v_5^2 - v_6^2 + v_5^2 - v_8^2 + v_7^2 - v_6^2 + v_7^2 - v_8^2}{16 \cdot g^2} \ldots (20)$$

$$\Rightarrow \bar{dg} \equiv \frac{\left(v_5^2 + v_7^2\right) - \left(v_6^2 + v_8^2\right)}{8 \cdot g^2}$$

All four RF envelope values v_k are used corresponding to IQ DC test vectors where k = [5,6,7,8]. We will demonstrate the method's error estimate extraction accuracy with an example (excessively high) IQ gain imbalance of *dg* = 0.05. This corresponds to a gain imbalance of +0.42 dB or -0.45 dB.

Worked Example with IQ gain error *dg* = 0.05;

k	V_{iq} Test Vector	V_{iq} with Gain Error	v_k^2	$\bar{dg} \equiv \frac{v_5^2 + v_7^2 - \left(v_6^2 + v_8^2\right)}{8 \cdot g^2}$
5	1+ j 0	1.05 + j 0	1.1025	
6	0 + j 1	0 + j 0.95	0.9025	
7	-1 + j 0	-1.05 + j 0	1.1025	
8	0 - j 1	0 - j 0.95	0.9025	***dg* = 0.05**

The estimate for IQ gain imbalance shows excellent accuracy. In practice other system imperfections such as DAC and ADC bit resolution may degrade this accuracy. The solution is to apply the correction iteratively. The IQ gain imbalance estimate is used to inversely scale the IQ signal voltages, resulting in a much lower “composite” IQ gain imbalance. The test vectors are then reapplied to this corrected system and a much lower IQ gain imbalance is obtained. The inverse of this new IQ gain imbalance is then multiplied by the previous IQ gain imbalance (or alternatively, *dg* can be updated incrementally until an acceptable convergence limit is achieved).

Note: A reasonably "good" Analog IQ modulator will have an IQ gain imbalance less ±0.1 dB, corresponding to a sideband suppression ration or -40 dB. The extremely poor IQ mixer used for this demonstration shows the estimation method to be extremely robust.

2.3. How to Estimate LO Phase Skew Errors Based On A Model Based Parameter Extraction Method.

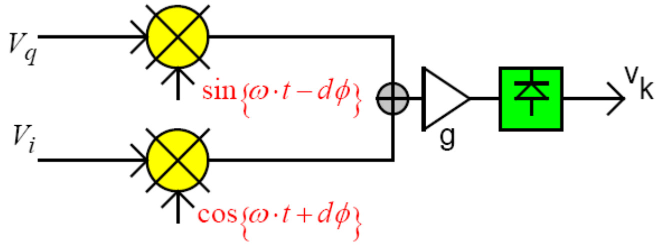
As mentioned previously, inexact quadrature LO phase phase also degrades in band SNR from cross coupled energy between upper and lower RF sideband spectral energy. It is not unreasonable to expect that an equivalent effect would be obtained by cross coupling I and Q signal energy presented to an "ideal" Analogue IQ Modulator without phase skew errors. We will represent this mechanism as a phase skew matrix operation that rotates I and Q axis' in opposite directions (i.e. not a rotation in which both axis rotate the same way!)

Analogue IQ Phase Skew Compensation

Phase skew errors are usually caused by inexact quadrature phase in the LO path for the IQ mixer. This phase skew mechanism will make a circular trajectory on a perfect IQ plane take on an elliptical path (i.e. not a rotation!)

IQ Phase Skew Error Referred to Baseband

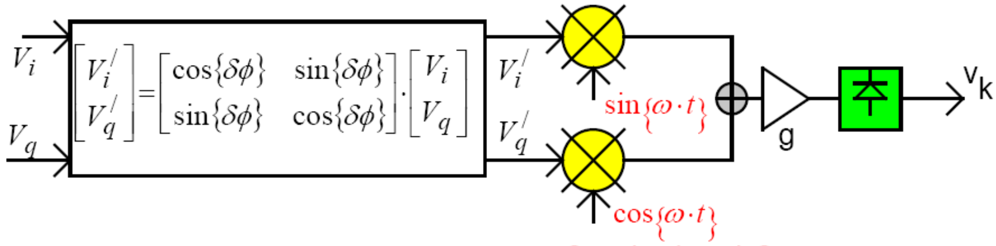
IQ Mixer with LO Phase Skew



Quadradure LO with Phase Skew Error

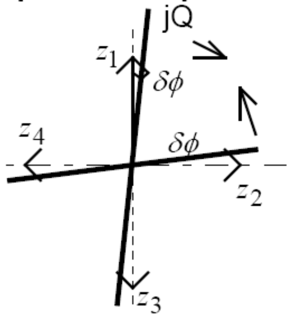
Equivalent Phase Skew At Baseband

"Perfect" IQ Mixer



Quadradure LO

Graphical Interpretation Of IQ Phase Skew Error



We can imagine the "imperfect" Analog IQ Mixer with a small internal phase error in it's LO input to be equivalent to a "perfect" Analog IQ mixer with this phase skew error introduced at IQ Baseband. This can be considered as "skewing" previously orthogonal I and Q axis' "skewed" so projections from vectors on these non orthogonal I' and Q' axes are no longer independant (cross coupled).

If FM or FSK is presented to such a mixer suffering from phase skew error, the output constellation will appear as an ellipse instead of a circle.

The equivalent (linear) distortion introduced at IQ Baseband from phase skew errors can be represented as a phase skew matrix operation,

$$\begin{bmatrix} V_i^{/} \\ V_q^{/} \end{bmatrix} = \begin{bmatrix} \cos\{\delta\phi\} & \sin\{\delta\phi\} \\ \sin\{\delta\phi\} & \cos\{\delta\phi\} \end{bmatrix} \cdot \begin{bmatrix} V_i \\ V_q \end{bmatrix} \ldots(21)$$

Expanding these terms out reveals,

$$\begin{aligned} v_k^2 &\equiv g^2 \cdot \left[(V_i \cdot \cos\{\delta\theta\} + V_q \cdot \sin\{\delta\theta\})^2 + (V_i \cdot \sin\{\delta\theta\} + V_q \cdot \cos\{\delta\theta\})^2 \right] \\ &= g^2 \cdot \left[(V_i^2 + V_q^2) \cdot (\cos^2\{\delta\theta\} + \sin^2\{\delta\theta\}) + 4 \cdot V_i \cdot V_q \cdot \cos\{\delta\theta\} \cdot \sin\{\delta\theta\}) \right] \ldots(22) \\ &i.e. \\ v_k^2 &= g^2 \cdot \left[\left(V_i^2 + V_q^2\right) + 4 \cdot V_i \cdot V_q \cdot \cos\{\delta\theta\} \cdot \sin\{\delta\theta\} \right] \end{aligned}$$

Once again we will define each test vector pair $V_{iq,k}$ and $V_{iq,k'}$ to have equal magnitude,

$$\left|V_{iq,k}\right| \equiv \left|V_{iq,k'}\right| \Rightarrow \left(V_{i,k}^2 + V_{q,k}^2\right) = \left(V_{i,k'}^2 + V_{q,k}^2\right) \ldots(23)$$

Then

$$\begin{aligned} &\Delta v_{k,k'}^2 = 4 \cdot g^2 \cdot \Delta V_{iq,k,k'} \cdot \cos\{\delta\theta\} \cdot \sin\{\delta\theta\} \\ &\textit{where } \Delta v_{k,k'}^2 \equiv v_k^2 - v_{k'}^2 \text{ and } \Delta V_{iq,k,k'} \equiv \left(V_{i,k} \cdot V_{q,k} - V_{i,k'} \cdot V_{q,k'}\right) \ldots(24) \\ &\Rightarrow \cos\{\delta\theta\} \cdot \sin\{\delta\theta\} = \frac{\Delta v_{k,k'}^2}{4 \cdot g^2 \cdot \Delta V_{iq,k,k'}} \end{aligned}$$

Given that the phase skew error is considered to be small (and tends to zero during the iterative correction training sequence) we can now approximate the trigonometric terms to be,

$$\cos\{\delta\theta\} \cdot \sin\{\delta\theta\} \cong \left(1 + \frac{1}{2} \cdot \delta\theta^2\right) \cdot \delta\theta \cong \delta\theta \text{ as } \delta\theta \to 0 \ldots(25)$$

The phase skew estimates then become,

$$\delta\theta \cong \frac{\Delta v_{k,k'}^2}{4 \cdot g^2 \cdot \Delta V_{iq,k,k'}} \ldots(25)$$

We will select test vector pairs with unit magnitude 1 but with V_i and V_q components of either sign. This implies,

The phase skew error is estimated from one pairing of IQ test vectors. However three other pairings are possible (in which the denominator is **not** equal to zero!).

$$V_{i,k} \cdot V_{q,k} \equiv V_{i,k'} \cdot V_{q,k'} \equiv \pm \frac{1}{2}$$
$$\Rightarrow \Delta V_{iq,k,k'} \in \begin{cases} 0 & same\ signs \\ \pm 1 & opposite\ signs \end{cases} \quad \ldots(26)$$

(Note the value of ±½ follows from this constraint in the test vector selection)

We will define 4 test vectors – as used in the IQ DC offset estimation method.

$$\begin{aligned} V_{iq,1} &= \frac{1}{\sqrt{2}} \cdot (1+j) \quad \Rightarrow V_{i,1} \cdot V_{q,1} = \tfrac{1}{2} \\ V_{iq,2} &= \frac{1}{\sqrt{2}} \cdot (1-j) \quad \Rightarrow V_{i,2} \cdot V_{q,2} = -\tfrac{1}{2} \\ V_{iq,3} &= \frac{1}{\sqrt{2}} \cdot (-1-j) \Rightarrow V_{i,3} \cdot V_{q,3} = \tfrac{1}{2} \\ V_{iq,4} &= \frac{1}{\sqrt{2}} \cdot (-1+j) \Rightarrow V_{i,4} \cdot V_{q,4} = -\tfrac{1}{2} \end{aligned} \quad \ldots(27)$$

We can now derive 4 estimates for the phase skew error from differences in these envelope values

$$\delta\theta \cong \frac{\Delta v_{1,2}^2}{4 \cdot g^2} = -\frac{\Delta v_{2,3}^2}{4 \cdot g^2} = \frac{\Delta v_{3,4}^2}{4 \cdot g^2} = -\frac{\Delta v_{4,1}^2}{4 \cdot g^2} \ldots(28)$$

We will now average all 4 phase skew estimates to obtain,

$$\delta\theta \cong \frac{\Delta v_{1,2}^2 + \Delta v_{3,4}^2 - \Delta v_{2,3}^2 - \Delta v_{4,1}^2}{16 \cdot g^2}$$
$$i.e. \quad \ldots(29)$$
$$\delta\theta \cong \frac{\left(v_1^2 + v_3^2\right) - \left(v_2^2 + v_4^2\right)}{8 \cdot g^2}$$

Once again the use of an average of all four estimates represents good engineering practice and leads to best expected phase skew error estimation accuracy. An example is now shown with a relatively high phase skew error of 3 degrees (1 degree is more typical in real IQ Modulators).

Worked Example with gain error $d\theta$ = 3° = 0.052360 radians

k	V_{iq} Test Vector	$v_k^2 = 1 \pm 0.10453$	$\bar{d\theta} \equiv \frac{\left(v_1^2 + v_3^2\right) - \left(v_2^2 + v_4^2\right)}{8 \cdot g^2}$	$\bar{d\theta}$ degrees $= \frac{360}{2 \cdot \pi} \cdot \bar{d\theta}$
1	0.707 + j 0.707	1.10453		0.05
2	0.707 – j 0.707	0.89547		0.05
3	-0.707 – j 0.707	1.10453		0.05
4	-0.707 + j 0.707	0.89547	0.052265	2.99456

From equation (22) with g = 1 we will have $v_k^2 = 1 + 4 \cdot V_i \cdot V_q \cdot \cos\{\delta\theta\} \cdot \sin\{\delta\theta\}$

Note: The phase skew error estimate is derived with excellent accuracy. It is standard practice to work with angular units in radians, but degrees are often more "comfortable" to conceptualize.

2.4. Summary Of All IQ Error Estimation Algorithms Based On A Model Based Parameter Extraction Process.

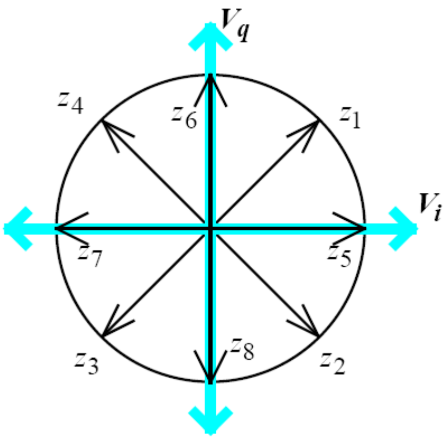
The 4 IQ error parameters are derived from this "Model Based Parameter Estimation" approach based on the use of 8 IQ test vectors and measurement of their corresponding RF output voltage magnitudes using a simple detector. The test vectors k=[1,2,3,4,5,6,7,8] can be applied in any order that is convenient and the corresponding RF envelope voltages stored as v_1, v_2 ,..., v_8 .

Summary

A family of 8 IQ test vectors has been presented with explanation for their selection. These test vectors allow Analogue IQ DC offset, gain imbalance and phase skew errors to be estimated with a simple RF envelope detector (e.g. diode). IQ errors are inferred from combinational values of these RF envelope voltages. The envelope perturbations, caused by the IQ errors, are predicted from a simple Analogue IQ modulator model (as opposed to a "blind" approach). This specific predictive knowledge provides extremely good error estimation accuracy therefore minimizing the number of iterations required for convergence.

This method uses 8 unit magnitude IQ test vectors (for convenience) but the exact value is somewhat arbitrary. These are spaced at adjacent rotations of 45 degrees.

Family of 8 Training Vectors z_k



Analogue IQ errors (IQ DC offset, gain imbalance, phase skew) produce predictable variations in the RF envelope for IQ voltages applied to a real IQ modulator with these error impairments. Therefore it is possible to predict these IQ error impairments by measuring these envelope variations.

Any test vector family can, in principle, be used. However, it is advantageous to use a test vector family that simplifies overall computational overhead. The test family presented here accomplishes this objective.

The family of 8 test vectors is presented to the Analogue IQ modulator in sequence. The RF envelope voltage (from a diode detector etc) is read for each and stored in memory. Specific combinations of these RF envelope voltages are then used to estimate each IQ error.

The "opposite" errors are then introduced digitally (e.g. DSP or FPGA implementation). The first iteration will remove most IQ inaccuracy. The test vector family is then reapplied with this correction applied. Remaining errors will be less, and the IQ correction is updated with the addition of these new values (e.g. standard iterative approach with a suitable step-size parameter).

Analogue IQ Error Estimation Table – RF Envelope Combinations Associated With Each IQ Test Vector Family

k	V_i	V_q	I DC Offset $\bar{\varepsilon}_i$	Q DC Offset $\bar{\varepsilon}_q$	Gain Imbalance $\bar{dg}$	Phase Skew $\bar{d\theta}$
1	$\frac{1}{\sqrt{2}}$	$\frac{1}{\sqrt{2}}$	$\frac{\left(v_1^2+v_2^2\right)-\left(v_3^2+v_4^2\right)}{4\cdot\sqrt{2}\cdot g^2}$	$\frac{\left(v_1^2+v_4^2\right)-\left(v_2^2+v_3^2\right)}{4\cdot\sqrt{2}\cdot g^2}$		$\frac{\left(v_1^2+v_3^2\right)-\left(v_2^2+v_4^2\right)}{8\cdot g^2}$
2	$\frac{1}{\sqrt{2}}$	$\frac{-1}{\sqrt{2}}$				
3	$\frac{-1}{\sqrt{2}}$	$\frac{-1}{\sqrt{2}}$				
4	$\frac{-1}{\sqrt{2}}$	$\frac{1}{\sqrt{2}}$				
5	1	0			$\frac{v_5^2+v_7^2-\left(v_6^2+v_8^2\right)}{8\cdot g^2}$	
6	0	1				
7	-1	0				
8	0	-1				

Note: The overall loop gain ratio g^2 is easily determined from $\bar{g}^2 \equiv \frac{1}{8}\cdot\sum_{k=1}^{8}\frac{v_k^2}{\left(V_{i,k}^2+V_{q,k}^2\right)}$. This gain scaling factor g does modify the value of each error estimate directly, but in a fairly benign linear way (It does not cause estimate corruption if it is inexact!). Its significance also diminishes as the IQ errors are reduced to zero during the iterative correction process. It is a useful procedure to apply in any case and provides a useful hardware diagnostic.

Analogue IQ Error Estimation Table – RF Envelope Combinations Associated With Each IQ Tes

k	V_i	V_q	I DC Offset $\bar{\varepsilon}_i$	Q DC Offset $\bar{\varepsilon}_q$	Gain Imbalance $\bar{dg}$	Ph
1	$\frac{1}{\sqrt{2}}$	$\frac{1}{\sqrt{2}}$	$\frac{\left(v_1^2+v_2^2\right)-\left(v_3^2+v_4^2\right)}{4\cdot\sqrt{2}\cdot g^2}$	$\frac{\left(v_1^2+v_4^2\right)-\left(v_2^2+v_3^2\right)}{4\cdot\sqrt{2}\cdot g^2}$		$(v$
2	$\frac{1}{\sqrt{2}}$	$\frac{-1}{\sqrt{2}}$				
3	$\frac{-1}{\sqrt{2}}$	$\frac{-1}{\sqrt{2}}$				
4	$\frac{-1}{\sqrt{2}}$	$\frac{1}{\sqrt{2}}$				
5	1	0			$\frac{v_5^2+v_7^2-\left(v_6^2+v_8^2\right)}{8\cdot g^2}$	
6	0	1				
7	-1	0				
8	0	-1				

Note: The overall loop gain ratio g^2 is easily determined from $\bar{g}^2 \equiv \frac{1}{8}\cdot\sum_{k=1}^{8}\frac{v_k^2}{\left(V_{i,k}^2+V_{q,k}^2\right)}$. This gain sca

value of each error estimate directly, but in a fairly benign linear way (It does not cause estimate significance also diminishes as the IQ errors are reduced to zero during the iterative correction proce apply in any case and provides a useful hardware diagnostic.

I hope this article helps people to achieve the optimum possible performance from Direct Conversion Transmitters based on Analog IQ Modulation. The hardware overhead for this IQ error estimation and correction method is minimal, comprising of a simple diode detector (high linearity is not essential and dynamic range requirements are extremely relaxed - the RF level input is always at a near constant level during training.)

The actual training ritual is best applied iteratively, even though the first iteration may provide near exact IQ error correction. The updated IQ error estimates, following each iteration, will show diminishing magnitude, tending to zero as convergence is achieved.

Without this correction, typical Analogue IQ modulators will exhibit LO carrier and sideband leakage between -35 and -40 dB. The correction obtained with the procedure described is usually better than -65 dB. This is clearly a massive improvement, and one that remains stable with time.

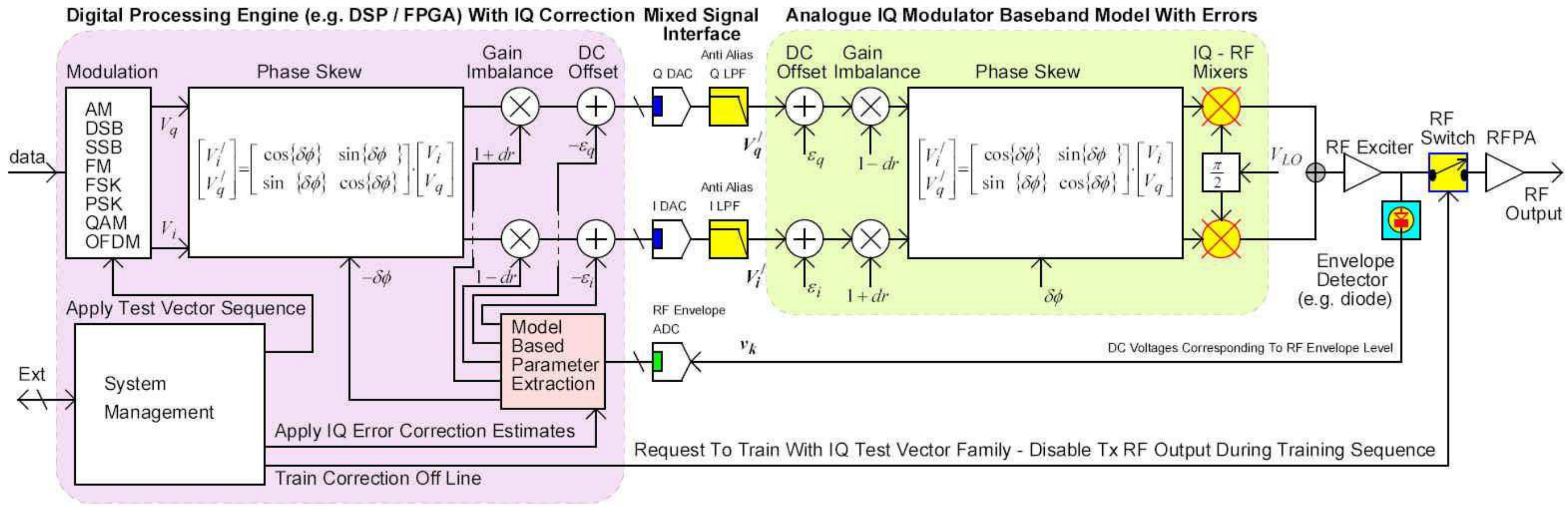
(I intend to describe a second method soon that avoids the need for off line test vectors. A simple diode envelope detector is still used but wider bandwidth and linearity requirements are assumed.)

Note: Even communication systems that require near 100% availability can still use "off line training" by sending Tx data in packets at a slightly faster rate than required to allow a time gap for training. A data buffer in the remote receiver would then simply supply continuous output data at the correct, slightly lower data rate. The only downside I see to this is the introduction of some data latency (i.e. delay in data throughput) but the acceptance limits on this depends on the actual application's latency requirement (no system can ever have zero latency as radio waves still have to travel at $3 \cdot 10^8$ m/s! - e.g. a separation of 50 km implies a path delay of 1.67 milliseconds anyway!).

3. Typical Direct Conversion Analogue IQ to RF Transmitter With IQ Error Correction.

These following diagrams show the overall architecture for a practical Direct Conversion Transmitter based on Analogue IQ Modulation combined with IQ error estimation and correction. This correction is applied "off line" during times when actual transmission of data is not required.

Complete Analogue IQ Modulator Concept With Model Based IQ Error Estimation and Correction ("Off Line" Correction Method Shown)



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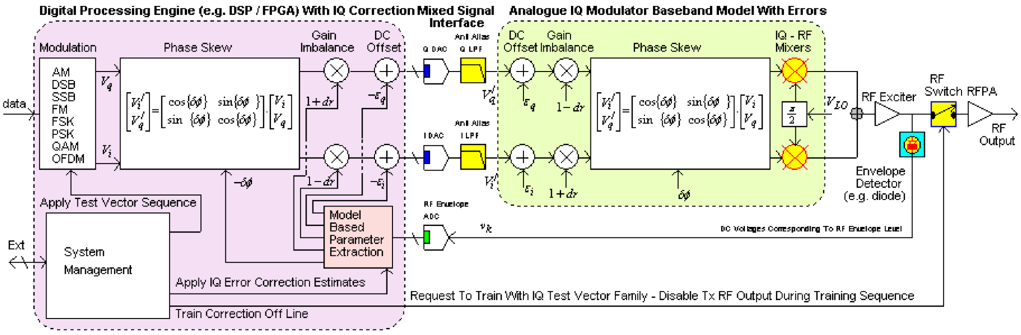

4. Using MATHCAD To Demonstrate Convergence Potential Using An Analogue IQ Modulator Baseband Model With IQ Errors

This MATHCAD file uses the previous 8 IQ Test Vectors with a slight modification where k = 0,1,...,7 instead of k = 1,2,...,8 as this suits matrix and array operations. The "AnalogIQ" function introduces IQ DC offset, IQ gain imbalance and IQ phase skew errors as equivalent complex Baseband error terms and produces a new distorted version of Viq corresponding to the introduction of these errors.

This AnalogIQ function is then called up in the "EstimateIQError" function. This compares the equivalent RF envelope voltage (that would be produced by a real imperfect Analog IQ modulator with these errors) against each IQ Test Vector as per the estimation procedure shown previously. These inferred IQ error estimates are transferred to the array "R".

Demonstrating The Effectiveness Of The Model Based IQ Error Estimation And Correction Algorithm Intended For Direct Conversion Transmitters Using An Analogue IQ to RF Modulator.

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Date of this Revision: 2 December, 2007

1. Introduction

This MATHCAD 7 File shows the convergence speed and accuracy for the IQ Error Estimation and Correction Algorithm I have presented in my latest web site. It is intended to show "effectiveness in principle" rather than direct application on a hardware platform (I don't have available hardware at this stage!). Therefore I have elected to use a "Model" to represent a DIrect Conversion transmitter using an imperfect IQ Modulator followed by some simple RF amplification (scale factor g)

The actual LO and RF frequencies are not relevant to this correction procedure, nor is the particular RF phase. A (scalar) RF envelope detector (i.e. a simple diode - responds only to RF amplitude and is insensitive to absolute phase) reports RF envelope voltages corresponding to a series of 8 pre-defined IQ test vectors. The relative combinations of these detected voltages, compared to the IQ test vectors allows IQ DC offset, IQ gain imbalance and LO phase skew errors to be inferred based on a Model Based interpretation (as described in my web discussion).

These IQ errors can then be used to "pre-distort" the IQ input signals intended for modulation so as to cancel out the effect of the Analogue IQ Modulator's interanl IQ errors.

This predistortion simply used the same Analog IQ Modulator Model "in reverse" with equal and opposite IQ errors derived from the error estimation procedure.

This MATHCAD file will show the massive correction potential that is possible with even relatively poor Analog IQ Modulators with relatively low computational overhead and a minimal number of training iterations. This procedure, in principle, removes the imperfections of Analogue IQ Modulator components from becoming the "weak link" in any Direct Conversion transmitter architecture.

2. IQ DC Test Vector Family of 8

A set of 8 IQ Test Vectors are used for training with this IQ error estimation and correction algorithm. These can be applied in any order - as long as each RF envelope voltage is paired correspondingly. Each training iteration uses these 8 IQ test vector applied as a set.

$$\mathrm{TestVectors} := \left[\left(\frac{1}{\sqrt{2}}+\frac{j}{\sqrt{2}}\right)\ \left(\frac{1}{\sqrt{2}}-\frac{j}{\sqrt{2}}\right)\ \left(-\frac{1}{\sqrt{2}}-\frac{j}{\sqrt{2}}\right)\ \left(-\frac{1}{\sqrt{2}}+\frac{j}{\sqrt{2}}\right)\ 1\ \ j\ \ -1\ \ -j\right]^T$$

Note - the Transpose operator is used used to produce a row of array values (sometimes more convenient)

3. Analogue IQ Modulator Model Referred To Equivalent IQ Baseband

This Analog IQ Modulator Model is presented as a "Baseband equivalent" model so that the LO and RF components can be discarded. It allows IQ DC offset errors, IQ gain imbalance and LO phase skew errors to be represented as "equivalent IQ errors". In other words, a real IQ modulator with internal IQ errors would present the same final RF output signal as a "perfect" IQ Modulator with an pre-distorted IQ input signal based on these IQ errors applied to this AnalogIQ model.

$$
\mathrm{AnalogIQ}(g, \varepsilon iq, \delta g, \delta\phi, Viq) := \left|
\begin{array}{l}
\mathrm{Samples} \leftarrow \mathrm{rows}(Viq) \\
\text{for } n \in 0..\mathrm{Samples}-1 \\
\quad \left|
\begin{array}{l}
Viq1 \leftarrow Viq_n + \varepsilon iq \\
Viq2 \leftarrow Viq1 + \delta g \cdot \overline{Viq1} \\
IQ \leftarrow \begin{bmatrix} \cos(\delta\phi) & \sin(\delta\phi) \\ \sin(\delta\phi) & \cos(\delta\phi) \end{bmatrix} \cdot \begin{bmatrix} \mathrm{Re}(Viq2) \\ \mathrm{Im}(Viq2) \end{bmatrix} \\
Viq3 \leftarrow IQ_0 + j \cdot IQ_1 \\
NewViq_n \leftarrow g \cdot Viq3
\end{array}\right. \\
NewViq
\end{array}\right.
$$

This "IQ Baseband Equivalent" model has an overall IQ to RF voltage conversion gain "g", an equivalent IQ DC offset input voltage $\varepsilon iq = \varepsilon i + j\ \varepsilon q$, IQ gain imbalance δg and phase skew error $\delta\phi$. The resulting output is in IQ Baseband format, corresponding to an equivalent IQ signal that could be presented to a "perfect" IQ modulator with unity gain and produce an identical RF output signal.

3. IQ Correction Model - Applying IQ Errors In The Opposite Order & "sign"

$$
\mathrm{IQCorrect}(\varepsilon iq, \delta g, \delta\phi, Viq) := \left|
\begin{array}{l}
\mathrm{Samples} \leftarrow \mathrm{rows}(Viq) \\
Viq \leftarrow Viq \\
\text{for } n \in 0..\mathrm{Samples}-1 \\
\quad \left|
\begin{array}{l}
A \leftarrow \begin{bmatrix} \cos(\delta\phi) & -\sin(\delta\phi) \\ -\sin(\delta\phi) & \cos(\delta\phi) \end{bmatrix} \\
IQ \leftarrow \begin{bmatrix} \cos(\delta\phi) & -\sin(\delta\phi) \\ -\sin(\delta\phi) & \cos(\delta\phi) \end{bmatrix} \cdot \begin{bmatrix} \mathrm{Re}\left(Viq_n\right) \\ \mathrm{Im}\left(Viq_n\right) \end{bmatrix} \\
Viq1 \leftarrow IQ_0 + j \cdot IQ_1 \\
Viq2 \leftarrow Viq1 - \delta g \cdot \overline{Viq1} \\
NewViq_n \leftarrow Viq2 - \varepsilon iq
\end{array}\right. \\
NewViq
\end{array}\right.
$$

The previous formula is described in my web article. The IQ correction errors are introduced in the reverse order to their generation in the Analog IQ Model. First, the IQ axis' phase skew error is removed with a matrix multiplication using the opposite phase skew argument in the cos{δφ} and sin{δφ} matrix entries. The relative IQ gain imbalance is then removed (note the $Viq1 - \delta g \cdot \overline{Viq1}$ is just "shorthand" for I * (1-δg), Q*(1+δg) i.e opposite as an approximation to I*(1+δg), Q*(1-δg)). The last step is to remove the IQ DC offset error based on the complex variable estimate εiq.

This correction includes two approximations - first the matrix should really be inverted so introducing 1/det(A) would help preserve overall conversion gain. The effect of leaving det(A) out is to cause the "corrected" IQ magnitude to be slightly less than the input IQ signal magnitude. The extent depends on the size of the phase skew error and is generally small (<< 0.2 dB reduction in overall conversion gain!)

Further, the IQ relative gain scale compensation should really be based on a division factor rather than simply I*(1+δg), Q*(1-δg). This has a small effect on conversion gain also. However the added computational overhead of taking an "exact" compensation approach is questionable. The actual IQ compensation accuracy is unaffected. The only consequence is that the IQ and Q input signal magnitudes may need to be scaled very slightly higher to compensate (and a typical power control loop suystem would be expected to be implemented for this anyway!)

I have included a more accurate version "IQCorrect2" so that people can test the difference for themselves!

$$
\mathrm{IQCorrect2}(\varepsilon iq, \delta g, \delta\phi, Viq) := \left|
\begin{array}{l}
\mathrm{Samples} \leftarrow \mathrm{rows}(Viq) \\
Viq \leftarrow Viq \\
\text{for } n \in 0..\mathrm{Samples}-1 \\
\quad \left|
\begin{array}{l}
A \leftarrow \begin{bmatrix} \cos(\delta\phi) & \sin(\delta\phi) \\ \sin(\delta\phi) & \cos(\delta\phi) \end{bmatrix} \\
IQ \leftarrow A^{-1} \cdot \begin{bmatrix} \mathrm{Re}\left(Viq_n\right) \\ \mathrm{Im}\left(Viq_n\right) \end{bmatrix} \\
Viq1 \leftarrow IQ_0 + j \cdot IQ_1 \\
Viq2 \leftarrow \dfrac{\mathrm{Re}(Viq1)}{1+\delta g} + j \cdot \dfrac{\mathrm{Im}(Viq1)}{1-\delta g} \\
NewViq_n \leftarrow Viq2 - \varepsilon iq
\end{array}\right. \\
NewViq
\end{array}\right.
$$

4. Cascading The IQ Compensation Model And IQ Analogue Modulator Model To Create An Overall "Composite Analog IQ Modulator" Model.

$$
\mathrm{CompositeIQ}(g, \varepsilon iq, \delta g, \delta\phi, \_\varepsilon iq, \_\delta g, \_\delta\phi, Viq) := \left|
\begin{array}{l}
NewViq \leftarrow \mathrm{IQCorrect}(\_\varepsilon iq, \_\delta g, \_\delta\phi, Viq) \\
\mathrm{AnalogIQ}(g, \varepsilon iq, \delta g, \delta\phi, NewViq)
\end{array}\right.
$$

5. Deriving IQ Error Estimates From The IQ Training Vector Sequence And The Reulting, Equivalent IQ Baseband Output.

Estimates for conversion gain "g", IQ DC offset error "εiq", relative IQ gain error "δg" and phase skew error "δϕ" are inferred from combinational values of equivalent rectified RF voltage associated with each of the 8 IQ Test Vectors (as shown in my article).

$$
\text{EstimateIQError}(TV, Viq) := \left|
\begin{array}{l}
\text{for } k \in 0..7 \\
\quad v_k \leftarrow 1 \cdot \left| Viq_k \right| \\
g2 \leftarrow \frac{1}{8} \cdot \sum_{k=0}^{7} \left(\frac{v_k}{\left\| TV_k \right\|} \right)^2 \\
\varepsilon i \leftarrow \frac{\left[(v_0)^2 + (v_1)^2 \right] - \left[(v_2)^2 + (v_3)^2 \right]}{4 \cdot \sqrt{2} \cdot g2} \\
\varepsilon q \leftarrow \frac{\left[(v_0)^2 + (v_3)^2 \right] - \left[(v_1)^2 + (v_2)^2 \right]}{4 \cdot \sqrt{2} \cdot g2} \\
\delta g \leftarrow \frac{\left[(v_4)^2 + (v_6)^2 \right] - \left[(v_5)^2 + (v_7)^2 \right]}{8 \cdot g2} \\
\delta \phi \leftarrow \frac{\left[(v_0)^2 + (v_2)^2 \right] - \left[(v_1)^2 + (v_3)^2 \right]}{8 \cdot g2} \\
R \leftarrow \left[\sqrt{g2} \quad \varepsilon i + j \cdot \varepsilon q \quad \delta g \quad \delta \phi \right]^T
\end{array}
\right.
$$

6. Defining an Iterative IQ Error Correction Training Sequence

No error estimate is ever exact on the first computation. It is reasonable therefore to apply an iterative approach in which IQ errors are successively reduced. Each IQ error has a starting value, assumed to be zero. These are then updated with a step parameter "Δ" which determines the rate of convergence, or instability if set too large (Δ should be less than 1, e.g. Δ=0.5 is a common value).

$$
\text{Train}(Iters, \Delta, g, \varepsilon iq, \delta g, \delta \phi, TV) := \left|
\begin{array}{l}
\_\varepsilon iq \leftarrow 0 \\
\_\delta g \leftarrow 0 \\
\_\delta \phi \leftarrow 0 \\
\text{for } i \in 0..Iters - 1 \\
\quad \left| \begin{array}{l}
Viq \leftarrow \text{CompositeIQ}(g, \varepsilon iq, \delta g, \delta \phi, \_\varepsilon iq, \_\delta g, \_\delta \phi, TV) \\
\Psi \leftarrow \text{EstimateIQError}(TV, Viq) \\
\_g \leftarrow \Psi_0 \\
\_\varepsilon iq \leftarrow \_\varepsilon iq + \Delta \cdot \Psi_1 \\
\_\delta g \leftarrow \_\delta g + \Delta \cdot \Psi_2 \\
\_\delta \phi \leftarrow \_\delta \phi + \Delta \cdot \Psi_3
\end{array} \right. \\
R^{\langle 0 \rangle} \leftarrow (20\,(\log(\_g) \quad \_\varepsilon iq \quad \_\delta g \quad \_\delta \phi)^T \\
R^{\langle 1 \rangle} \leftarrow \left[20 \left(\log\left(\frac{\_g}{g} \right) \right. \quad \left| \varepsilon iq - \_\varepsilon iq \right| \quad \delta g - \_\delta g \quad \delta \phi - \_\delta \phi \right]^T \\
R
\end{array}
\right.
$$

Note: I use the underscore "_" prefix to distinguish between an error estimate and the original, introduced error value.

The array R has two columns and 4 rows. The first column contains estated conversion gain (expressed in dB), Complex IQ DC offset error εi + j εq, gain imbalance δg and phase skew δϕ.

The second column contains the difference between the actual introduced error and the estimates obtained from the iterative procedure.

The number of Iterations is contained in the variable "Iters".

7. Introducing Initial IQ Errors (Relatively Extreme For Demonstration)

$g := 3$	Overall voltage gain from |Viq| to Vrf envelope voltage
$\varepsilon iq := 0.1 - j \cdot 0.05$	I and Q DC offset voltages expressed as I + j*Q complex form
$\delta g := 0.07$	Relative IQ gain imbalance expressed as 1+δg, 1-δg
$\delta \phi := -0.085$	$\frac{360}{2 \cdot \pi} \cdot \delta \phi = -4.87$ Phase skew error in radians and then in degrees

8. Demonstrating The Iterative Error Estimation and Correction Process

$\Delta := 0.9$ Stepsize of increment

Iterations = 1 — Estimate, Error in Estimate

$$\mathrm{Train}(1,\Delta,g,\varepsilon iq,\delta g,\delta\phi,\mathrm{TestVectors}) = \begin{bmatrix} 9.629 & 0.087 \\ 0.108 - 0.053i & 8.946\cdot10^{-3} \\ 0.062 & 8.247\cdot10^{-3} \\ -0.074 & -0.011 \end{bmatrix} \begin{matrix} \text{Conversion Gain in dB} \\ \text{IQ DC Offset Voltage} \\ \text{IQ Linear gain Imbalance } dg \\ \text{IQ Phase Skew in radians} \end{matrix}$$

Note: Good early IQ error estimation

Iterations = 5 — Estimate, Error in Estimate

$$\mathrm{Train}(5,\Delta,g,\varepsilon iq,\delta g,\delta\phi,\mathrm{TestVectors}) = \begin{bmatrix} 9.374 & -0.169 \\ 0.1 - 0.05i & 1.372\cdot10^{-6} \\ 0.07 & 3.835\cdot10^{-7} \\ -0.085 & -6.325\cdot10^{-7} \end{bmatrix} \begin{matrix} \text{Conversion Gain in dB} \\ \text{IQ DC Offset Voltage} \\ \text{IQ Linear gain Imbalance } dg \\ \text{IQ Phase Skew in radians} \end{matrix}$$

Note: Excellent IQ error estimation after just 5 iterations!

Iterations = 10 — Estimate, Error in Estimate

$$\mathrm{Train}(10,\Delta,g,\varepsilon iq,\delta g,\delta\phi,\mathrm{TestVectors}) = \begin{bmatrix} 9.374 & -0.169 \\ 0.1 - 0.05i & 3.083\cdot10^{-10} \\ 0.07 & 1.452\cdot10^{-12} \\ -0.085 & -3.123\cdot10^{-12} \end{bmatrix} \begin{matrix} \text{Conversion Gain in dB} \\ \text{IQ DC Offset Voltage} \\ \text{IQ Linear gain Imbalance } dg \\ \text{IQ Phase Skew in radians} \end{matrix}$$

Note: Exceptional IQ error estimation after 10 iterations!

Iterations = 50 — Estimate, Error in Estimate

$$\mathrm{Train}(50,\Delta,g,\varepsilon iq,\delta g,\delta\phi,\mathrm{TestVectors}) = \begin{bmatrix} 9.374 & -0.169 \\ 0.1 - 0.05i & 0 \\ 0.07 & 0 \\ -0.085 & 0 \end{bmatrix} \begin{matrix} \text{Conversion Gain in dB} \\ \text{IQ DC Offset Voltage} \\ \text{IQ Linear gain Imbalance } dg \\ \text{IQ Phase Skew in radians} \end{matrix}$$

Note: Looks like the job is all done after 50 iterations! Note the small residual loss in output level - a gain drop of -0.169 dB caused by the approaximations used in the procedure. This is clearly insignificant and correctable by simple scaling.

Some arbitrary IQ errors are introduced and the "EstimateIQError" algorithm was used to infer them. The first iterations were quite successful. Further iterations showed significant improvement. The IQ errors were rapidly estimated with extremely good accuracy.

Consequently the use of an "off line" IQ error estimation and correction procedure does not appear to be problematic. Its key features are,

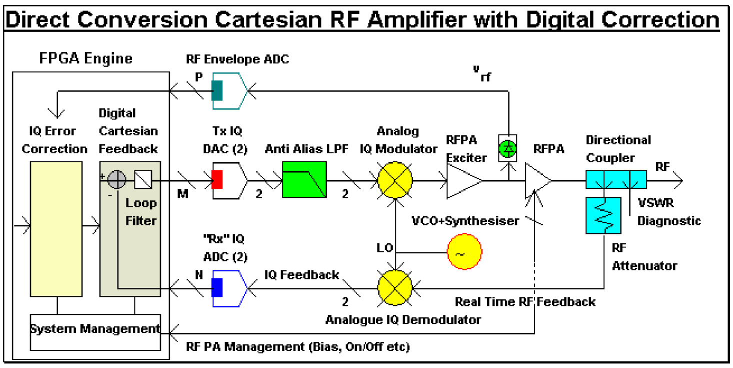
- Its hardware implementation has low cost and complexity
- The need for periodic "retraining" is unlikely as these errors tend to remain quite stable over time, and show slight variation over temperature extremes.
- The number of iterations required for convergence is small - perhaps 5 or less. If each iteration takes as long as 1 millisecond, the transmitter only needs to be "offline" for 5 milliseconds to perform the IQ error correction ritual.

If the transmitter cannot afford to be "offline" for any period, e.g. as may be a constraint required of a critical microwave data link, then Analog IQ modulation can still be used but a slight modification to the approach is called for. I hope to publish this method soon (on this web site!). However it may well be easier to just use the use of a receiver buffer and send data slightly faster than required to leave a training gap as suggested earlier.

This more generic method uses the IQ values "as is" to represent test vectors, and the envelope variations are compared with these IQ values to infer IQ errors in real time, on line.

5. Potential Application To RF Power Amplifier Linearisation With Cartesian Feedback (Narrow Band System)

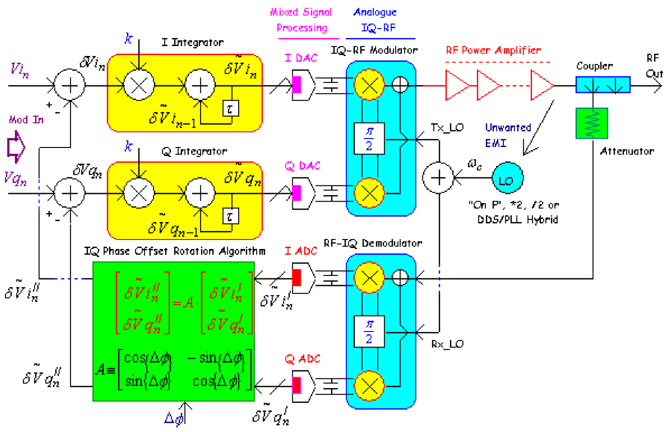
Analog IQ modulation is often associated with RF PA linearisation based on a "Cartesian Feedback" approach. This architecture is most suited for narrow bandwidth modulation formats such as TETRA DQPSK or TR8.12 "Tetrapol" FSK.



Negative Feedback is applied at IQ Baseband, as opposed to the actual RF frequency. The comparison between forward (Tx) and reverse (Rx) IQ paths can be performed with analog components, or in the digital domain (as shown). The digital approach allows any phase offset correction to be applied digitally - avoiding the need for an extra Analog LO phase rotation component.

A Cartesian linearisation architecture based on Analog IQ/RF Up and Down conversion, combined with digitally implemented phase rotation and negative feedback with a simple loop filter (for stability) can be represented as follows,

General Cartesian Loop RF Power Amplifier Linearization Sub System



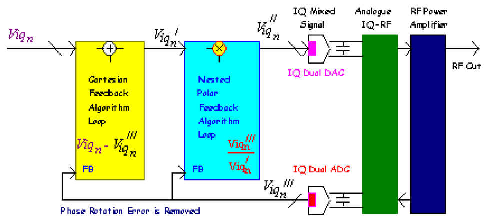
This architecture is very suitable for narrow band technologies such as those used in PMR (Public Mobile Radio) applications. This includes TETRA DQPSK Modulation and "Tetrapol" TR8.12 Modulation Formats. These modulation formats typically have spectral bandwidth requirements of about 20 kHz. The mixed signal devices (ADC and DAC) still require medium to high sample rates (e.g. 40 MHz or higher) in order to allow a high effective "open loop bandwidth" so that ample loop gain is available within the IQ modulation bandwidth for non linearity correction caused by RF Power Amplifier artifacts. The ADC "latency", i.e. how many clock cycles are needed to transfer an acquired signal to its digital output bus, is also important and this loop delay time limits the unity gain bandwidth.

In practice, a closed loop unity gain bandwidth 300 kHz or greater is possible, and Adjacent Channel Sideband Power (ACP) reductions of 15 to 20 dB are readily attained with medium cost components.

The concept can be enhanced (almost indefinitely) by using a "nested loop approach". This places a Cartesian Corrected RF PA loop inside an outer Cartesian Corrected RF PA loop, thereby extending the correction potential for non linear artifacts. (This approach of nested loops is common practice in audio amplifier design!). Of course the loops do not all need to be Cartesian - here is an example of a Polar Feedback system enclosed in an outer Cartesian Feedback correction loop.

Nested Polar Loop Inside Cartesian Loop Linearization Sub System

Potential ACP Advantage Is Twice That Of Single Feedback Loop



Additional "outer loops" can be added if required. The ultimate correction potential depends on the IQ Demodulator performance. Since this is placed in the feedback, any distortion introduced by the IQ demodulator will show up on the RF output. The simplest solution is to run this component at a reduced RF input level so that its linearity improves.

Then the IQ error correction procedure may become more relevant as IQ DC offset errors will become more significant compared to a reduced IQ output signal level.

Still, I hope this article shows the wide relevance that Analogue RF/IQ device technology has to radio communication systems. The Direct Conversion architecture is a personal favorite of mine, and can benefit greatly from enhancement processing implemented in the digital domain (DSP or FPGA devices). Unfortunately not all radio product manufacturers are aware of these error estimation and correction algorithms (or perhaps any?). Perhaps this article will help to shed some light on methods suitable for Direct Conversion performance enhancement.

6. Example Analogue IQ Modulator IC's

Several companies have invested significant R&D resource into the development of high performance Analog IQ Modulator IC's. Although originally spanned by passive diode based component offerings, these components have largely lost favor in the industry due to excessive cost and mediocre IQ performance. They also tend to have relatively low RF operating bandwidth. IC implementations, in contrast, are usually far superior in all aspects.

STQ-2016 IQ Modulator IC From Sirenza / Acquired by RFMD

STQ-2016(Z)

800-2500 MHz Direct Quadrature Modulator

Product Features

- 800-2500MHz Operating Frequency
- No External IF Filter
- Very Low Noise Floor Performance
- Excellent Carrier and Sideband Suppression
- Shutdown Feature
- Low LO Drive Requirements
- Single 5.0V Supply
- Supports Wideband Baseband Input

Product Applications

- Cellular/PCS/DCS/3G Transceivers
- GMSK, QPSK, QAM, SSB Modulators
- Digital Communication Systems
- ISM Band Transceivers
- Spread Spectrum Communication Systems

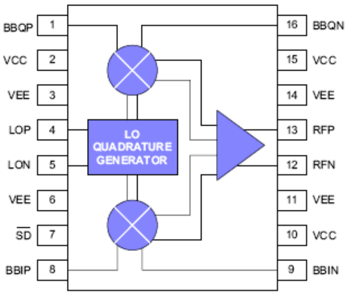
Product Images


Product Image

Product Parameters

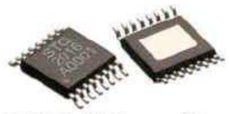
Baseband	DC-500 MHz
Carrier Feedthrough	-40 dBm
Id	73 mA
P1dB	3.0 dBm
RF/LO	700-2500 MHz
Sideband Suppression	40 dBm
Vd	5.0 V

Functional Block Diagram



STQ-2016
STQ-2016Z RoHS Compliant & Green Package

700-2500 MHz Direct Quadrature Modulator



16 pin TSSOP with Exposed Ground Pad
Package Footprint: 0.197 x 0.252 inches, (5.0 x 6.4 mm)
Package Height: 0.039 inches (1.0 mm)

Product Features

- **Excellent carrier feedthrough, -40 dBm constant with output power**
- **Output P1dB +3dBm**
- **Wide baseband input, DC - 500 MHz**
- **Superb phase accuracy and amplitude balance, ±0.5 deg./±0.2 dB**
- **Very low noise floor, -155 dBm/Hz**
- **Low LO drive requirement, -5 dBm**

Linear Technology - LT5518 & LT5572 Analogue IQ Modulators

LT5518 - 1.5GHz2.4GHz High Linearity Direct Quadrature Modulator

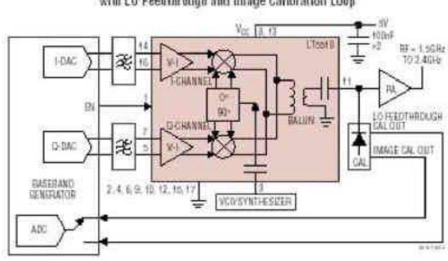
FEATURES | DESCRIPTION | PACKAGING | APPLICATIONS | SIMULATE

FEATURES

- High Input Impedance Version of the LT5528
- Direct Conversion to 1.5GHz - 2.4GHz
- High OIP3: 22.8dBm at 2GHz
- Low Output Noise Floor at 20MHz Offset:
- No RF: -158.2dBm/Hz
- P_{OUT} = 4dBm: -152.5dBm/Hz
- 4-Ch W-CDMA ACPR: -64dBc at 2.14GHz
- Integrated LO Buffer and LO Quadrature Phase Generator
- 50Ω AC-Coupled Single-Ended LO and RF Ports
- Low Carrier Leakage: -49dBm at 2GHz
- High Image Rejection: 40dB at 2GHz
- 16-Lead QFN 4mm × 4mm Package

TYPICAL APPLICATION

1.5GHz to 2.4GHz Direct Conversion Transmitter Application with LO Feedthrough and Image Calibration Loop



LT5572 - 1.5GHz to 2.5GHz High Linearity Direct Quadrature Modulator

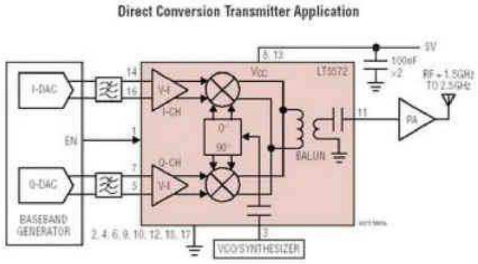
FEATURES | DESCRIPTION | PACKAGING | APPLICATIONS | SIMULATE

FEATURES

- Direct Conversion from Baseband to RF
- High Output: –2.5dB Conversion Gain
- High OIP3: +21.6dBm at 2GHz
- Low Output Noise Floor at 20MHz Offset:
  - No RF: –158.6dBm/Hz
  - P_{OUT} = 4dBm: –152.5dBm/Hz
- Low Carrier Leakage: –39.4dBm at 2GHz
- High Image Rejection: –41.2dBc at 2GHz
- 4-Channel W-CDMA ACPR: –67.7dBc at 2.14GHz
- Integrated LO Buffer and LO Quadrature Phase Generator
- 50Ω AC-Coupled Single-Ended LO and RF Ports
- High Impedance DC Interface to Baseband Inputs with 0.5V Common Mode Voltage
- 16-Lead QFN 4mm × 4mm Package

TYPICAL APPLICATION

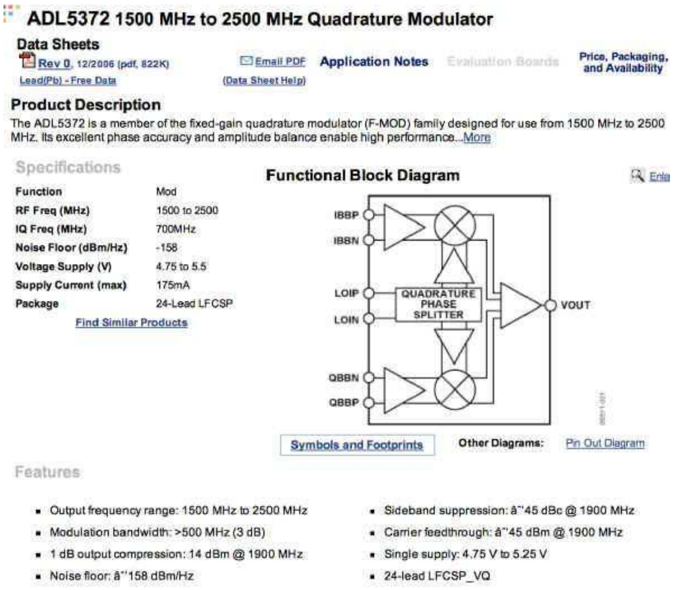
Direct Conversion Transmitter Application



Note: The LT5518 application shows the use of a diode detector for IQ error correction - but there is **no need** for a dual output! It appears that Linear Technology is ***unaware*** of the much simpler IQ error estimation and correction procedure I have just described!

They do make great RF IC's though!

Analog Devices ADL5372 Analog IQ Modulator


ADL5372 1500 MHz to 2500 MHz Quadrature Modulator

Data Sheets

Rev 0, 12/2006 (pdf, 822K) | Email PDF | Application Notes | Evaluation Boards | Price, Packaging, and Availability

Lead(Pb) - Free Data | (Data Sheet Help)

Product Description

The ADL5372 is a member of the fixed-gain quadrature modulator (F-MOD) family designed for use from 1500 MHz to 2500 MHz. Its excellent phase accuracy and amplitude balance enable high performance...More

Specifications

Function	Mod
RF Freq (MHz)	1500 to 2500
IQ Freq (MHz)	700MHz
Noise Floor (dBm/Hz)	-158
Voltage Supply (V)	4.75 to 5.5
Supply Current (max)	175mA
Package	24-Lead LFCSP

Find Similar Products

Functional Block Diagram

Symbols and Footprints | Other Diagrams: Pin Out Diagram

Features

- Output frequency range: 1500 MHz to 2500 MHz
- Modulation bandwidth: >500 MHz (3 dB)
- 1 dB output compression: 14 dBm @ 1900 MHz
- Noise floor: â''158 dBm/Hz
- Sideband suppression: â''45 dBc @ 1900 MHz
- Carrier feedthrough: â''45 dBm @ 1900 MHz
- Single supply: 4.75 V to 5.25 V
- 24-lead LFCSP_VQ

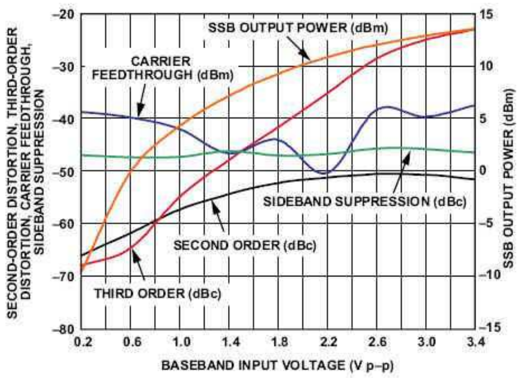
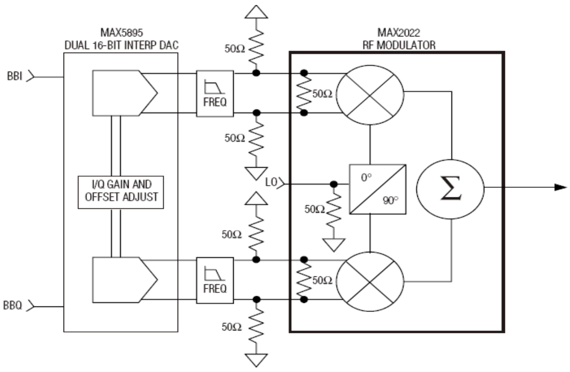
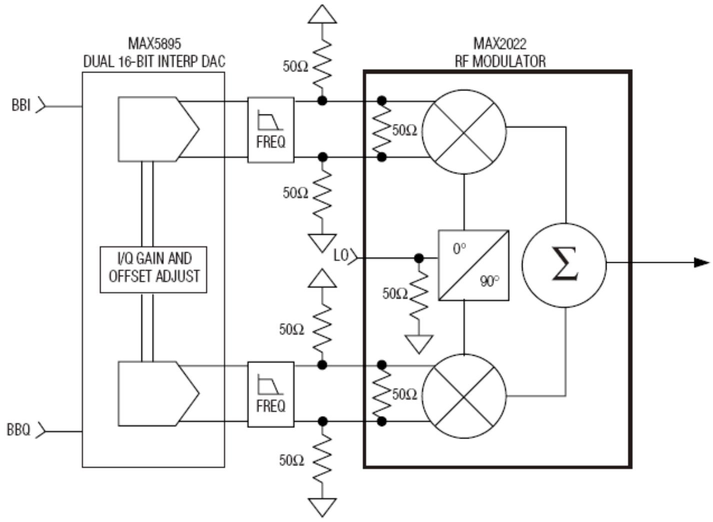


Figure 14. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. Baseband Differential Input Level (f_{LO} = 1900 MHz)

Maxim-IC MAX2022 Analogue IQ Modulator





Note: The use of a direct DAC to IQ interface is a great bonus! This usually requires a center IQ input voltage equal to 0.5 V.

Return to: Analog IQ

or: Ian Scotts Technology Pages